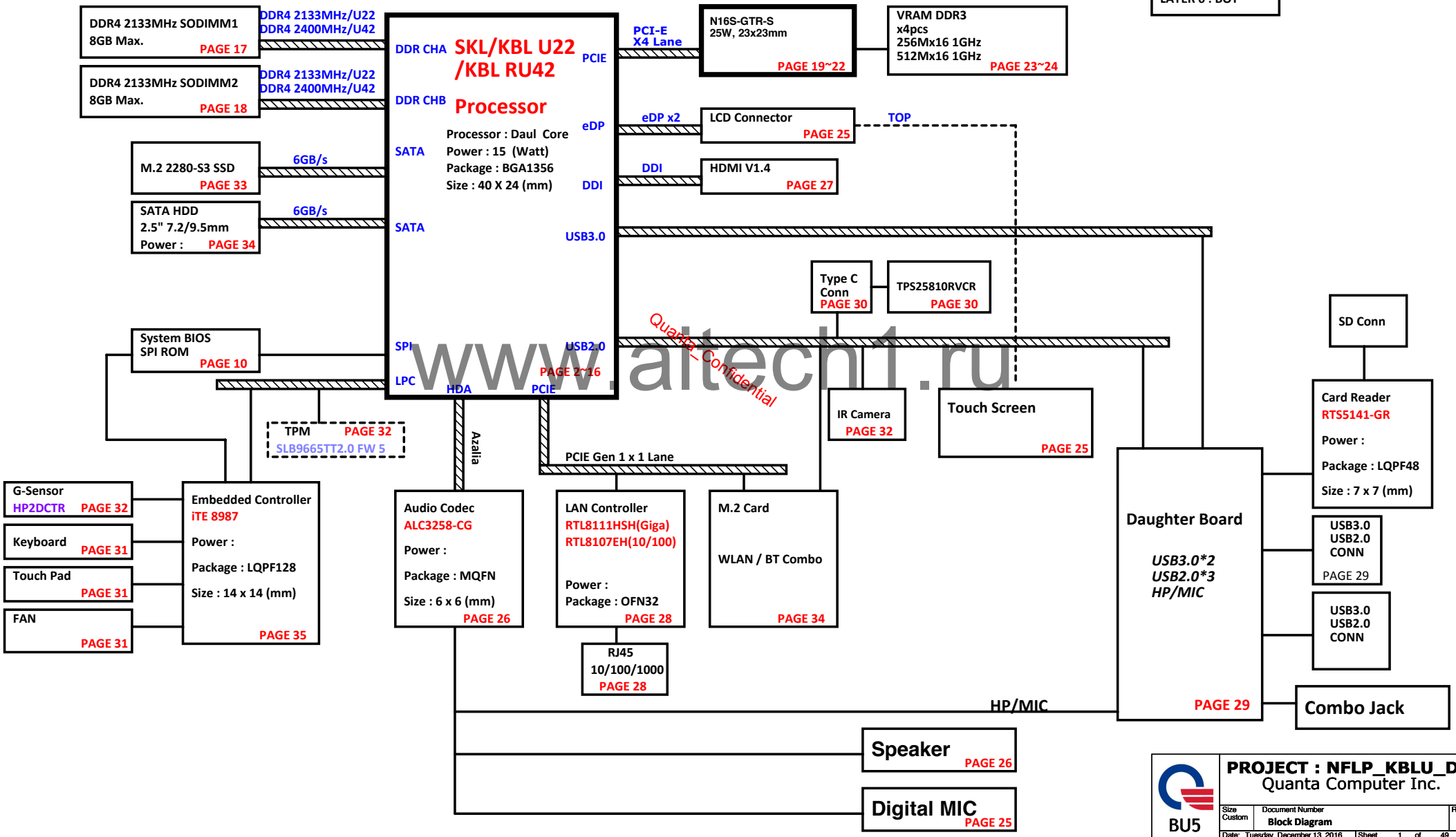
NFL_1SPD DIS (14/15")
Intel SKL/KBL ULT Platform Block Diagram

01

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT



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PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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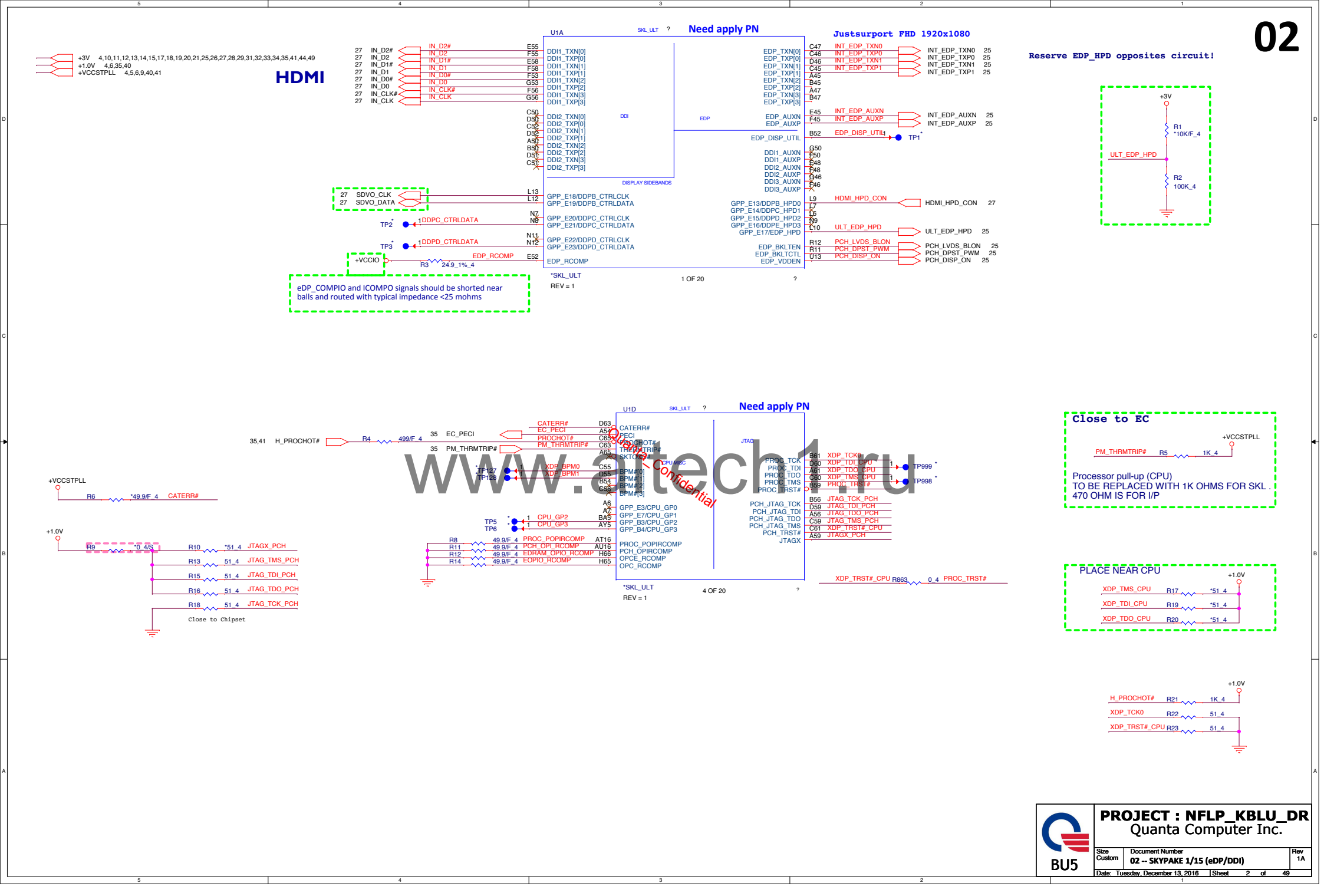

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

BU5

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/15 (eDP/DDI)	1A

Date: Tuesday, December 13, 2016 Sheet 2 of 49

SkyLake ULT Processor (DDR4)

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.2VSUS 6,17,18,38,40,46

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U1B SKL_ULT

M_A_DQ0	AL71	DDR0_DQ[0]		AU53	M_A_CLKN0 17
M_A_DQ1	AL68	DDR0_DQ[1]	DDR0_CKN[0]	AT53	M_A_CLKP0 17
M_A_DQ2	AN68	DDR0_DQ[2]	DDR0_CKP[0]	AU55	M_A_CLKN1 17
M_A_DQ3	AN69	DDR0_DQ[3]	DDR0_CKN[1]	AT55	M_A_CLKP1 17
M_A_DQ4	AL70	DDR0_DQ[4]	DDR0_CKP[1]		
M_A_DQ5	AL69	DDR0_DQ[5]	DDR0_CKE[0]	BA56	M_A_CKE0 17
M_A_DQ6	AN70	DDR0_DQ[6]	DDR0_CKE[1]	BB56	M_A_CKE1 17
M_A_DQ7	AN71	DDR0_DQ[7]	DDR0_CKE[2]	AW56	
M_A_DQ8	AR70	DDR0_DQ[8]	DDR0_CKE[3]	AY56	
M_A_DQ9	AR68	DDR0_DQ[9]	DDR0_CS#[0]	AU45	M_A_CS#0 17
M_A_DQ10	AU71	DDR0_DQ[10]	DDR0_CS#[1]	AU43	M_A_CS#1 17
M_A_DQ11	AU68	DDR0_DQ[11]	DDR0_ODT[0]	AT45	M_A_DIM0_ODT0 17
M_A_DQ12	AR71	DDR0_DQ[12]	DDR0_ODT[1]	AT43	M_A_DIM0_ODT1 17
M_A_DQ13	AR69	DDR0_DQ[13]			
M_A_DQ14	AU70	DDR0_DQ[14]	DDR0_MA[5]/DDR0_CAA(0)/DDR0_MA[5]	BA51 M_A_A5	M_A_A5 17
M_A_DQ15	AU69	DDR0_DQ[15]	DDR0_MA[9]/DDR0_CAA(1)/DDR0_MA[9]	BB54 M_A_A9	M_A_A9 17
M_B_DQ0	AF65	DDR1_DQ[0]/DDR0_DQ[16]	DDR0_MA[6]/DDR0_CAA(2)/DDR0_MA[6]	AY52 M_A_A6	M_A_A6 17
M_B_DQ1	AF64	DDR1_DQ[1]/DDR0_DQ[17]	DDR0_MA[8]/DDR0_CAA(3)/DDR0_MA[8]	AW52 M_A_A7	M_A_A8 17
M_B_DQ2	AK65	DDR1_DQ[2]/DDR0_DQ[18]	DDR0_MA(7)/DDR0_CAA(4)/DDR0_MA(7)	AY55 M_A_BG#0	M_A_A7 17
M_B_DQ3	AK64	DDR1_DQ[3]/DDR0_DQ[19]	DDR0_BA(2)/DDR0_CAA(5)/DDR0_BG(0)	AW54 M_A_A12	M_A_BG#0 17
M_B_DQ4	AF68	DDR1_DQ[4]/DDR0_DQ[20]	DDR0_MA(12)/DDR0_CAA(6)/DDR0_MA(12)	BA54 M_A_A11	M_A_A12 17
M_B_DQ5	AF67	DDR1_DQ[5]/DDR0_DQ[21]	DDR0_MA(11)/DDR0_CAA(7)/DDR0_MA(11)	BA55	M_A_A11 17
M_B_DQ6	AK67	DDR1_DQ[6]/DDR0_DQ[22]	DDR0_MA(15)/DDR0_CAA(8)/DDR0_ACT#	AY54	M_A_ACT# 17
M_B_DQ7	AK66	DDR1_DQ[7]/DDR0_DQ[23]	DDR0_MA(14)/DDR0_CAA(9)/DDR0_BG(1)		M_A_BG#1 17
M_B_DQ8	AF70	DDR1_DQ[8]/DDR0_DQ[24]		AU46 M_A_A13	M_A_A13 17
M_B_DQ9	AF68	DDR1_DQ[9]/DDR0_DQ[25]	DDR0_MA(13)/DDR0_CAB(0)/DDR0_MA(13)	AU48	M_A_CAS# 17
M_B_DQ10	AH71	DDR1_DQ[10]/DDR0_DQ[26]	DDR0_CAS#/DDR0_CAB(1)/DDR0_MA(15)	AT46	M_A_WE# 17
M_B_DQ11	AH68	DDR1_DQ[11]/DDR0_DQ[27]	DDR0_WE#/DDR0_CAB(2)/DDR0_MA(14)	AU50	M_A_RAS# 17
M_B_DQ12	AF71	DDR1_DQ[12]/DDR0_DQ[28]	DDR0_RAS#/DDR0_CAB(3)/DDR0_MA(16)	AU52	M_A_BS#0 17
M_B_DQ13	AF69	DDR1_DQ[13]/DDR0_DQ[29]	DDR0_BA(0)/DDR0_CAB(4)/DDR0_BA(0)	AY51 M_A_A2	M_A_A2 17
M_B_DQ14	AH70	DDR1_DQ[14]/DDR0_DQ[30]	DDR0_MA(2)/DDR0_CAB(5)/DDR0_MA(2)	AT48	M_A_BS#1 17
M_B_DQ15	AH69	DDR1_DQ[15]/DDR0_DQ[31]	DDR0_BA(1)/DDR0_CAB(6)/DDR0_BA(1)	AT50 M_A_A10	M_A_A10 17
M_A_DQ16	BB65	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_MA(10)/DDR0_CAB(7)/DDR0_MA(10)	BB50 M_A_A1	M_A_A1 17
M_A_DQ17	AW65	DDR0_DQ[17]/DDR0_DQ[33]	DDR0_MA(1)/DDR0_CAB(8)/DDR0_MA(1)	AY50 M_A_A0	M_A_A0 17
M_A_DQ18	AW63	DDR0_DQ[18]/DDR0_DQ[34]	DDR0_MA(0)/DDR0_CAB(9)/DDR0_MA(0)	BA50 M_A_A3	M_A_A3 17
M_A_DQ19	AY63	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_MA[3]	BB52 M_A_A4	M_A_A4 17
M_A_DQ20	BA65	DDR0_DQ[20]/DDR0_DQ[36]	DDR0_MA[4]		
M_A_DQ21	AY65	DDR0_DQ[21]/DDR0_DQ[37]		AM70 M_A_DQSN0	
M_A_DQ22	BA63	DDR0_DQ[22]/DDR0_DQ[38]	DDR0_DQSN[0]	AM69 M_A_DQSP0	
M_A_DQ23	BB63	DDR0_DQ[23]/DDR0_DQ[39]	DDR0_DQSP[0]	AT69 M_A_DQSN1	
M_A_DQ24	BA61	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_DQSN[1]	AT70 M_A_DQSP1	
M_A_DQ25	AW61	DDR0_DQ[25]/DDR0_DQ[41]	DDR0_DQSP[1]	AH66 M_B_DQSN0	
M_A_DQ26	BB59	DDR0_DQ[26]/DDR0_DQ[42]	DDR1_DQSN[0]/DDR0_DQSN[2]	AH65 M_B_DQSP0	
M_A_DQ27	AW59	DDR0_DQ[27]/DDR0_DQ[43]	DDR1_DQSP[0]/DDR0_DQSP[2]	AG69 M_B_DQSN1	
M_A_DQ28	BB61	DDR0_DQ[28]/DDR0_DQ[44]	DDR1_DQSN[1]/DDR0_DQSN[3]	AG70 M_B_DQSP1	
M_A_DQ29	AY61	DDR0_DQ[29]/DDR0_DQ[45]	DDR1_DQSP[1]/DDR0_DQSP[3]	BA64 M_A_DQSN2	
M_A_DQ30	BA59	DDR0_DQ[30]/DDR0_DQ[46]	DDR0_DQSN[2]/DDR1_DQSN[4]	AY64 M_A_DQSP2	
M_A_DQ31	AY59	DDR0_DQ[31]/DDR0_DQ[47]	DDR0_DQSP[2]/DDR1_DQSP[4]	AY60 M_A_DQSN3	
M_B_DQ16	AT66	DDR1_DQ[16]/DDR0_DQ[48]	DDR0_DQSN[3]/DDR0_DQSN[5]	BA60 M_A_DQSP3	
M_B_DQ17	AU66	DDR1_DQ[17]/DDR0_DQ[49]	DDR0_DQSP[3]/DDR0_DQSP[5]	AR65 M_B_DQSN2	
M_B_DQ18	AP65	DDR1_DQ[18]/DDR0_DQ[50]	DDR1_DQSN[2]/DDR0_DQSN[6]	AR66 M_B_DQSP2	
M_B_DQ19	AN65	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_DQSP[2]/DDR0_DQSP[6]	AR61 M_B_DQSN3	
M_B_DQ20	AN66	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_DQSN[3]/DDR0_DQSN[7]	AR60 M_B_DQSP3	
M_B_DQ21	AP66	DDR1_DQ[21]/DDR0_DQ[53]	DDR1_DQSP[3]/DDR0_DQSP[7]		
M_B_DQ22	AT65	DDR1_DQ[22]/DDR0_DQ[54]			
M_B_DQ23	AU65	DDR1_DQ[23]/DDR0_DQ[55]	DDR0_ALERT#	AW50 M_A_ALERT#	M_A_ALERT# 17
M_B_DQ24	AT61	DDR1_DQ[24]/DDR0_DQ[56]	DDR0_PAR	AT52 M_A_PARITY	M_A_PARITY 17
M_B_DQ25	AU61	DDR1_DQ[25]/DDR0_DQ[57]			
M_B_DQ26	AP60	DDR1_DQ[26]/DDR0_DQ[58]	DDR_VREF_CA	AY67 SM_VREF	SM_VREF 17
M_B_DQ27	AN60	DDR1_DQ[27]/DDR0_DQ[59]	DDR0_VREF_DQ	AY68 SMDDR_VREF_DQ0_M3	TP7
M_B_DQ28	AN61	DDR1_DQ[28]/DDR0_DQ[60]	DDR1_VREF_DQ	BA67 SMDDR_VREF_DQ1_M3	SMDDR_VREF_DQ1_M3 18
M_B_DQ29	AP61	DDR1_DQ[29]/DDR0_DQ[61]			
M_B_DQ30	AT60	DDR1_DQ[30]/DDR0_DQ[62]	DDR_VTT_CNTL	AW67 DDR_VTT_CNTL	DDR_VTT_CNTL 18
M_B_DQ31	AU60	DDR1_DQ[31]/DDR0_DQ[63]			

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20mils width

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REV = 1
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U1C SKL_ULT

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M_A_DQ32	AY39	DDR0_DQ[32]/DDR1_DQ[0]		AN45	M_B_CLKN0 18
M_A_DQ33	AW39	DDR0_DQ[33]/DDR1_DQ[1]	DDR1_CKN[0]	AN46	M_B_CLKN1 18
M_A_DQ34	AY37	DDR0_DQ[34]/DDR1_DQ[2]	DDR1_CKP[0]	AP45	M_B_CLKP0 18
M_A_DQ35	AW37	DDR0_DQ[35]/DDR1_DQ[3]	DDR1_CKP[1]	AP46	M_B_CLKP1 18
M_A_DQ36	BB39	DDR0_DQ[36]/DDR1_DQ[4]			
M_A_DQ37	BA39	DDR0_DQ[37]/DDR1_DQ[5]	DDR1_CKE[0]	AN56	M_B_CKE0 18
M_A_DQ38	BA37	DDR0_DQ[38]/DDR1_DQ[6]	DDR1_CKE[1]	AP55	M_B_CKE1 18
M_A_DQ39	BB37	DDR0_DQ[39]/DDR1_DQ[7]	DDR1_CKE[2]	AN55	
M_A_DQ40	AY35	DDR0_DQ[40]/DDR1_DQ[8]	DDR1_CKE[3]	AP53	
M_A_DQ41	AW35	DDR0_DQ[41]/DDR1_DQ[9]			
M_A_DQ42	AY33	DDR0_DQ[42]/DDR1_DQ[10]	DDR1_CS#[0]	BB42	M_B_CS#0 18
M_A_DQ43	AW33	DDR0_DQ[43]/DDR1_DQ[11]	DDR1_CS#[1]	AY42	M_B_CS#1 18
M_A_DQ44	BB35	DDR0_DQ[44]/DDR1_DQ[12]	DDR1_ODT[0]	BA42	M_B_DIM0_ODT0 18
M_A_DQ45	BA35	DDR0_DQ[45]/DDR1_DQ[13]	DDR1_ODT[1]	AW42	M_B_DIM0_ODT1 18
M_A_DQ46	BA33	DDR0_DQ[46]/DDR1_DQ[14]			
M_A_DQ47	BB33	DDR0_DQ[47]/DDR1_DQ[15]	DDR1_MA[5]/DDR1_CAA(0)/DDR1_MA[5]	AY48 M_B_A5	M_B_A5 18
M_B_DQ32	AU40	DDR1_DQ[32]/DDR1_DQ[16]	DDR1_MA[9]/DDR1_CAA(1)/DDR1_MA[9]	AP50 M_B_A9	M_B_A9 18
M_B_DQ33	AT40	DDR1_DQ[33]/DDR1_DQ[17]	DDR1_MA[6]/DDR1_CAA(2)/DDR1_MA[6]	BA48 M_B_A8	M_B_A6 18
M_B_DQ34	AT37	DDR1_DQ[34]/DDR1_DQ[18]	DDR1_MA[8]/DDR1_CAA(3)/DDR1_MA[8]	BB48 M_B_A6	M_B_A8 18
M_B_DQ35	AU37	DDR1_DQ[35]/DDR1_DQ[19]	DDR1_MA(7)/DDR1_CAA(4)/DDR1_MA(7)	AP48 M_B_A8	M_B_A7 18
M_B_DQ36	AR40	DDR1_DQ[36]/DDR1_DQ[20]	DDR1_BA(2)/DDR1_CAA(5)/DDR1_BG(0)	AP52 M_B_A7	M_B_BG#0 18
M_B_DQ37	AP40	DDR1_DQ[37]/DDR1_DQ[21]	DDR1_MA(12)/DDR1_CAA(6)/DDR1_MA(12)	AN50 M_B_A12	M_B_A12 18
M_B_DQ38	AP37	DDR1_DQ[38]/DDR1_DQ[22]	DDR1_MA(11)/DDR1_CAA(7)/DDR1_MA(11)	AN48 M_B_A11	M_B_A11 18
M_B_DQ39	AR37	DDR1_DQ[39]/DDR1_DQ[23]	DDR1_MA(15)/DDR1_CAA(8)/DDR1_ACT#	AN53 M_B_ACT#	M_B_ACT# 18
M_B_DQ40	AT33	DDR1_DQ[40]/DDR1_DQ[24]	DDR1_MA(14)/DDR1_CAA(9)/DDR1_BG(1)	AN52 M_B_BG#1	M_B_BG#1 18
M_B_DQ41	AU33	DDR1_DQ[41]/DDR1_DQ[25]			
M_B_DQ42	AU30	DDR1_DQ[42]/DDR1_DQ[26]	DDR1_MA(13)/DDR1_CAB(0)/DDR1_MA[13]	BA43 M_B_A13	M_B_A13 18
M_B_DQ43	AT30	DDR1_DQ[43]/DDR1_DQ[27]	DDR1_CAS#/DDR1_CAB(1)/DDR1_MA[15]	AY43	M_B_CAS# 18
M_B_DQ44	AR33	DDR1_DQ[44]/DDR1_DQ[28]	DDR1_WE#/DDR1_CAB(2)/DDR1_MA[14]	AY44	M_B_WE# 18
M_B_DQ45	AP33	DDR1_DQ[45]/DDR1_DQ[29]	DDR1_RAS#/DDR1_CAB(3)/DDR1_MA[16]	AW44	M_B_RAS# 18
M_B_DQ46	AR30	DDR1_DQ[46]/DDR1_DQ[30]	DDR1_BA(0)/DDR1_CAB(4)/DDR1_BA(0)	BB44	M_B_BS#0 18
M_B_DQ47	AP30	DDR1_DQ[47]/DDR1_DQ[31]	DDR1_MA(2)/DDR1_CAB(5)/DDR1_MA(2)	AY47 M_B_A2	M_B_A2 18
M_A_DQ48	AY31	DDR1_DQ[48]/DDR1_DQ[32]	DDR1_BA(1)/DDR1_CAB(6)/DDR1_BA(1)	BA44	M_B_BS#1 18
M_A_DQ49	AW31	DDR1_DQ[49]/DDR1_DQ[33]	DDR1_MA(10)/DDR1_CAB(7)/DDR1_MA(10)	AW46 M_B_A10	M_B_A10 18
M_A_DQ50	AY29	DDR1_DQ[50]/DDR1_DQ[34]	DDR1_MA(1)/DDR1_CAB(8)/DDR1_MA(1)	AY46 M_B_A1	M_B_A1 18
M_A_DQ51	AW29	DDR1_DQ[51]/DDR1_DQ[35]	DDR1_MA(0)/DDR1_CAB(9)/DDR1_MA(0)	BB46 M_B_A0	M_B_A0 18
M_A_DQ52	BB31	DDR1_DQ[52]/DDR1_DQ[36]	DDR1_MA[3]	BA46 M_B_A3	M_B_A3 18
M_A_DQ53	BA31	DDR1_DQ[53]/DDR1_DQ[37]	DDR1_MA[4]	BA47 M_B_A4	M_B_A4 18
M_A_DQ54	BA29	DDR1_DQ[54]/DDR1_DQ[38]			
M_A_DQ55	BB29	DDR1_DQ[55]/DDR1_DQ[39]	DDR0_DQSN[4]/DDR1_DQSN[0]	BA38 M_A_DQSN4	
M_A_DQ56	AY27	DDR1_DQ[56]/DDR1_DQ[40]	DDR0_DQSP[4]/DDR1_DQSP[0]	AY38 M_A_DQSP4	
M_A_DQ57	AW27	DDR1_DQ[57]/DDR1_DQ[41]	DDR0_DQSN[5]/DDR1_DQSN[1]	AY34 M_A_DQSN5	
M_A_DQ58	AY25	DDR1_DQ[58]/DDR1_DQ[42]	DDR0_DQSP[5]/DDR1_DQSP[1]	BA34 M_A_DQSP5	
M_A_DQ59	AW25	DDR1_DQ[59]/DDR1_DQ[43]	DDR1_DQSN[4]/DDR1_DQSN[2]	AT38 M_B_DQSN4	
M_A_DQ60	BB27	DDR1_DQ[60]/DDR1_DQ[44]	DDR1_DQSP[4]/DDR1_DQSP[2]	AR38 M_B_DQSP4	
M_A_DQ61	BA27	DDR1_DQ[61]/DDR1_DQ[45]	DDR1_DQSN[5]/DDR1_DQSN[3]	AT32 M_B_DQSN5	
M_A_DQ62	BA25	DDR1_DQ[62]/DDR1_DQ[46]	DDR1_DQSP[5]/DDR1_DQSP[3]	AR32 M_B_DQSP5	
M_A_DQ63	BB25	DDR1_DQ[63]/DDR1_DQ[47]	DDR0_DQSN[6]/DDR1_DQSN[4]	BA30 M_A_DQSN6	
M_B_DQ48	AU27	DDR1_DQ[48]	DDR0_DQSP[6]/DDR1_DQSP[4]	AY30 M_A_DQSP6	
M_B_DQ49	AT27	DDR1_DQ[49]	DDR0_DQSN[7]/DDR1_DQSN[5]	AY26 M_A_DQSN7	
M_B_DQ50	AT25	DDR1_DQ[50]	DDR0_DQSP[7]/DDR1_DQSP[5]	BA26 M_A_DQSP7	
M_B_DQ51	AU25	DDR1_DQ[51]	DDR1_DQSN[6]	AR25 M_B_DQSN6	
M_B_DQ52	AP27	DDR1_DQ[52]	DDR1_DQSP[6]	AR27 M_B_DQSP6	
M_B_DQ53	AN27	DDR1_DQ[53]	DDR1_DQSN[7]	AR22 M_B_DQSN7	
M_B_DQ54	AN25	DDR1_DQ[54]	DDR1_DQSP[7]	AR21 M_B_DQSP7	
M_B_DQ55	AP25	DDR1_DQ[55]			
M_B_DQ56	AT22	DDR1_DQ[56]	DDR1_ALERT#	AN43 M_B_ALERT#	M_B_ALERT# 18
M_B_DQ57	AU22	DDR1_DQ[57]	DDR1_PAR	AP43 M_B_PARITY	M_B_PARITY 18
M_B_DQ58	AU21	DDR1_DQ[58]	DRAM_RESET#	AT13 SM_DRAMRST#	DDR3_DRAMRST# 17,18
M_B_DQ59	AT21	DDR1_DQ[59]	DDR_RCOMP[0]	AR18 SM_RCOMP_0	R25 121/F_4
M_B_DQ60	AN22	DDR1_DQ[60]	DDR_RCOMP[1]	AT18 SM_RCOMP_1	R26 80.6/F_4
M_B_DQ61	AP22	DDR1_DQ[61]	DDR_RCOMP[2]	AU18 SM_RCOMP_2	R27 100/F_4
M_B_DQ62	AP21	DDR1_DQ[62]			
M_B_DQ63	AN21	DDR1_DQ[63]			

NIL-DDR CH - B

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R24 470/F_4

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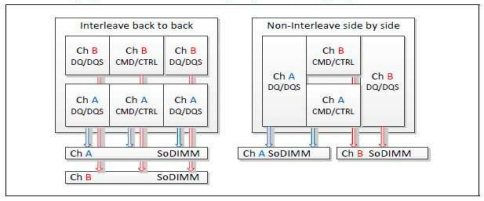
Interleave (IL) and Non-Interleave (NIL) Modes Mapping



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BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size Custom	Document Number 03 -- SKYLAKE 2/15(DDR4 I/F)	Rev 1A
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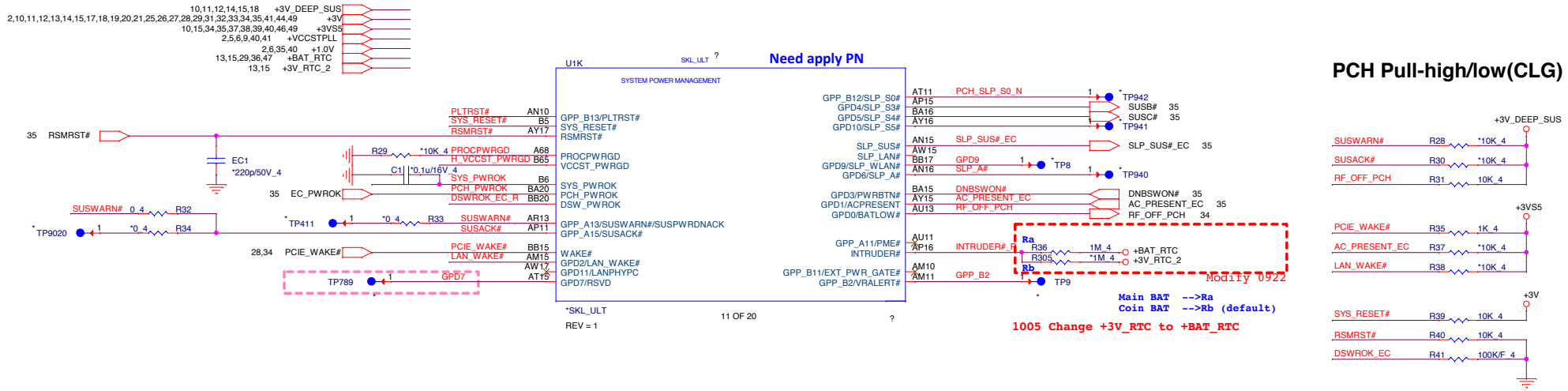
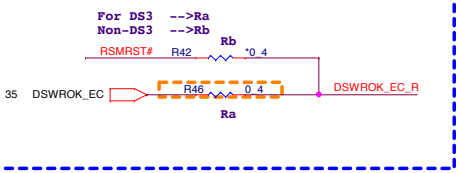


PCH Pull-high/low(CLG)

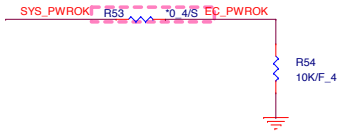
For DS3 Sequence

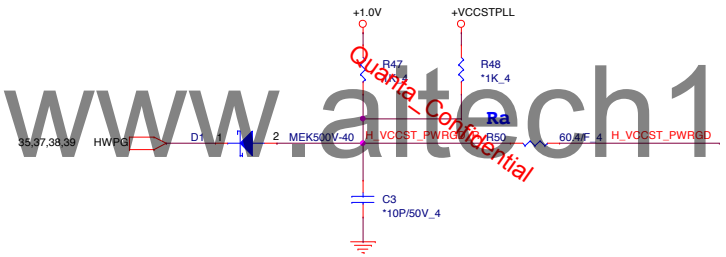


PLTRST#(CLG)

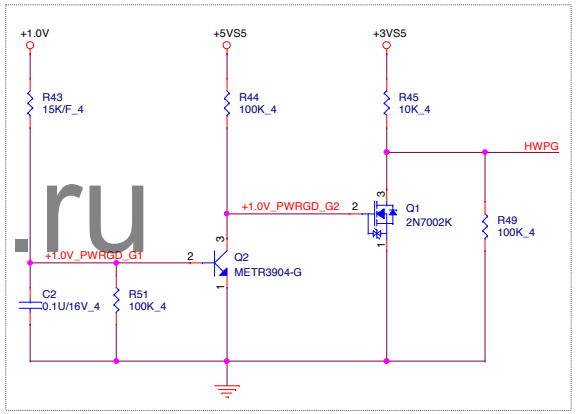
Check Rise/Fall time less than 100ns

System PWR_OK(CLG)





Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



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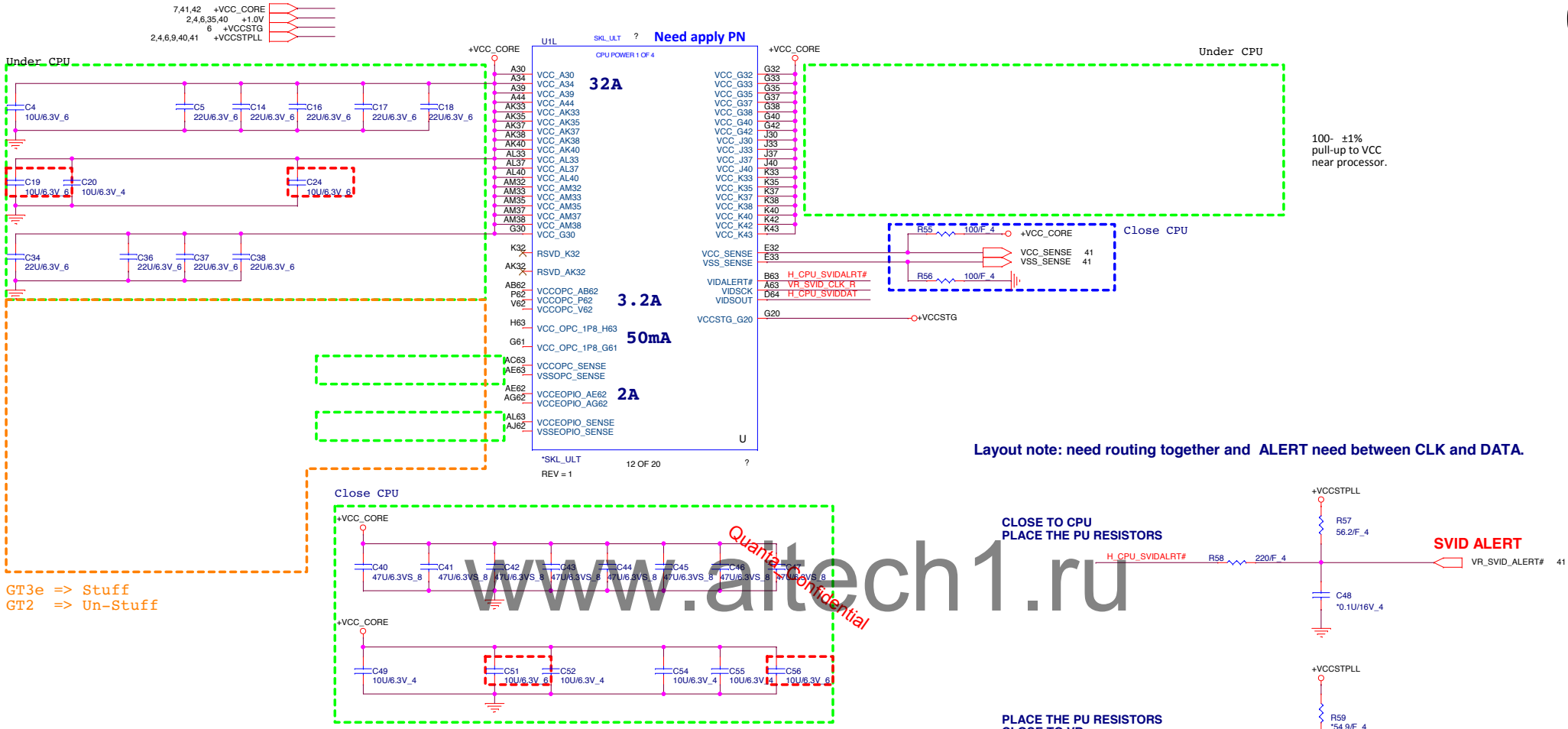
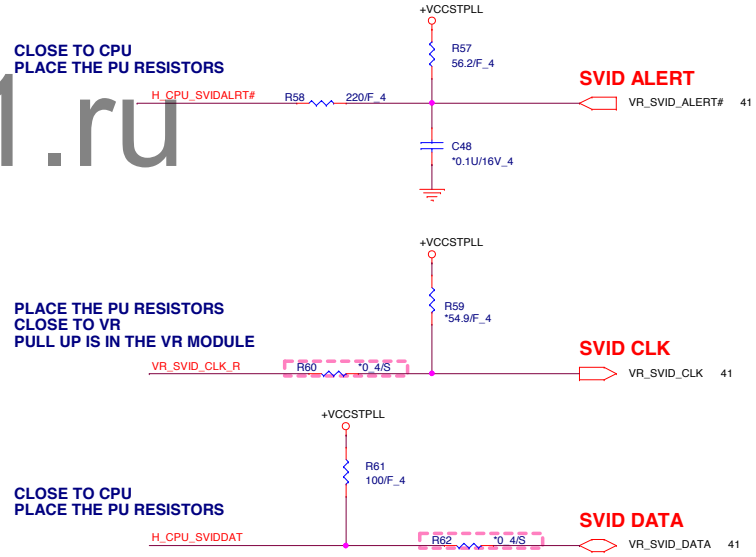
BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size Custom	Document Number **04 -- SKYLAKE 3/15(PowerManger)**	Rev 1A
Date: Tuesday, December 13, 2016	Sheet 4 of 49	



Layout note: need routing together and ALERT need between CLK and DATA.



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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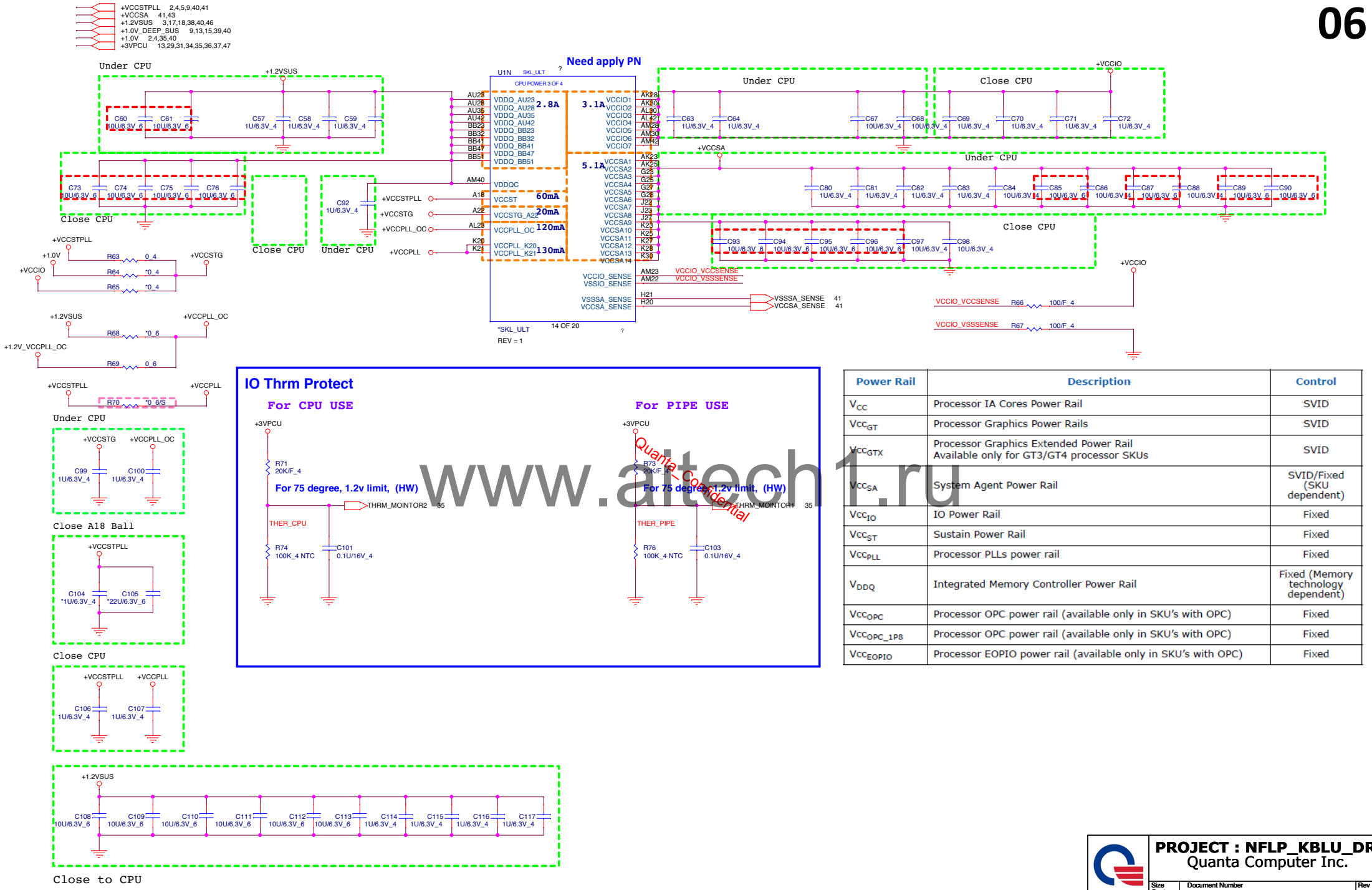
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYLAKE 4/15 (POWER-1)	1A

Date: Tuesday, December 13, 2016 Sheet 5 of 49



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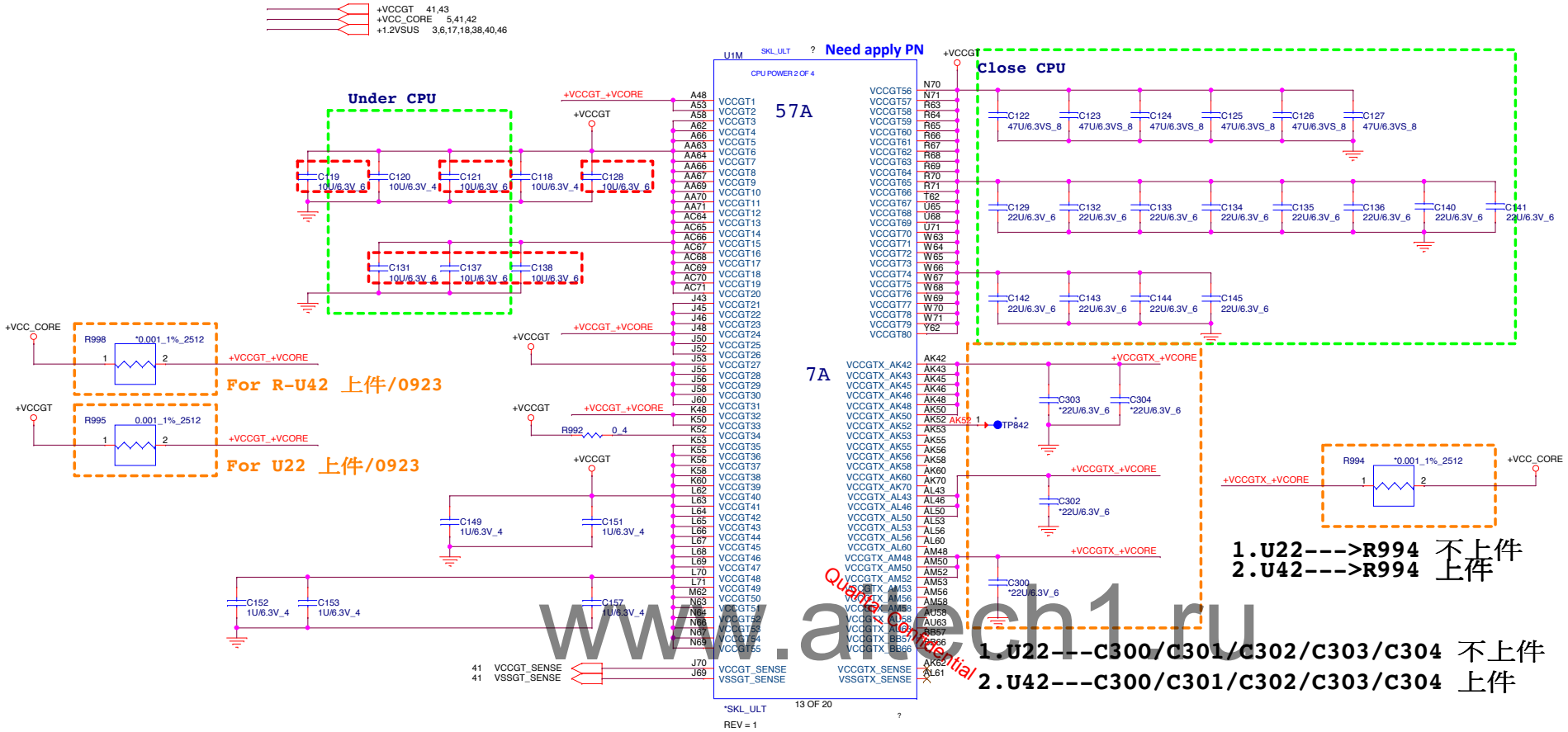
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



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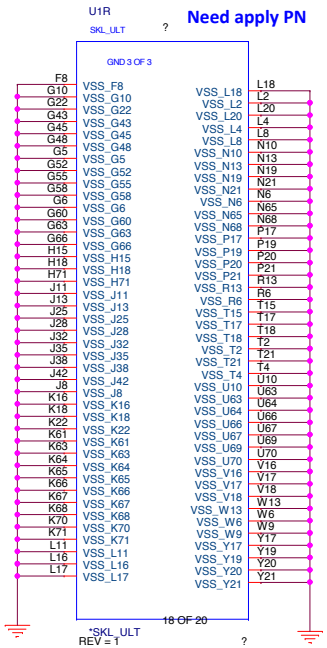
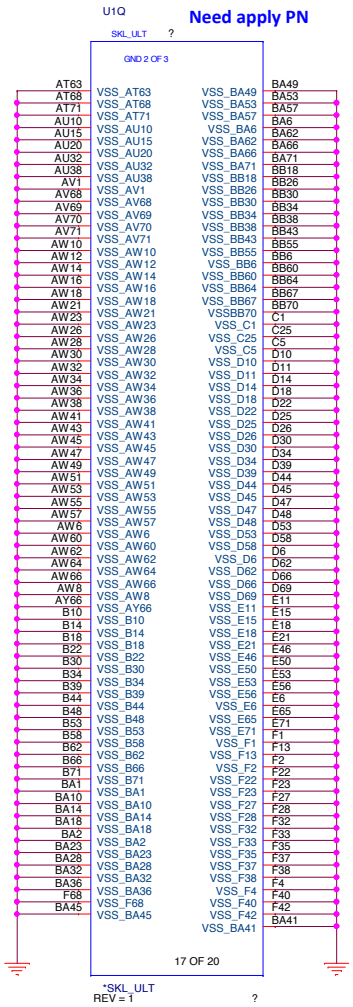
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed





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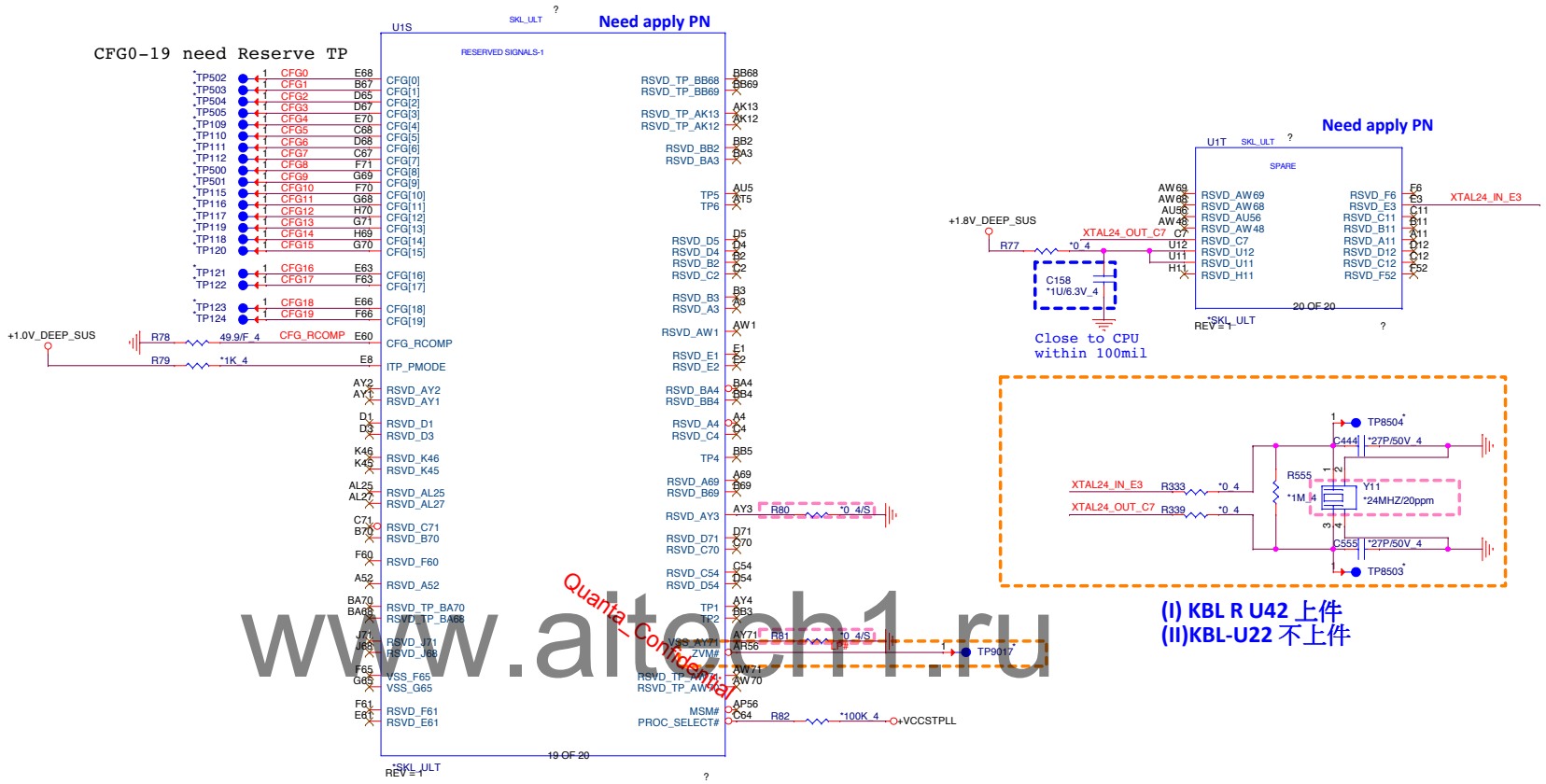
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE 7/15 (GND)	1A

Date: Tuesday, December 13, 2016 | Sheet 8 of 49



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Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

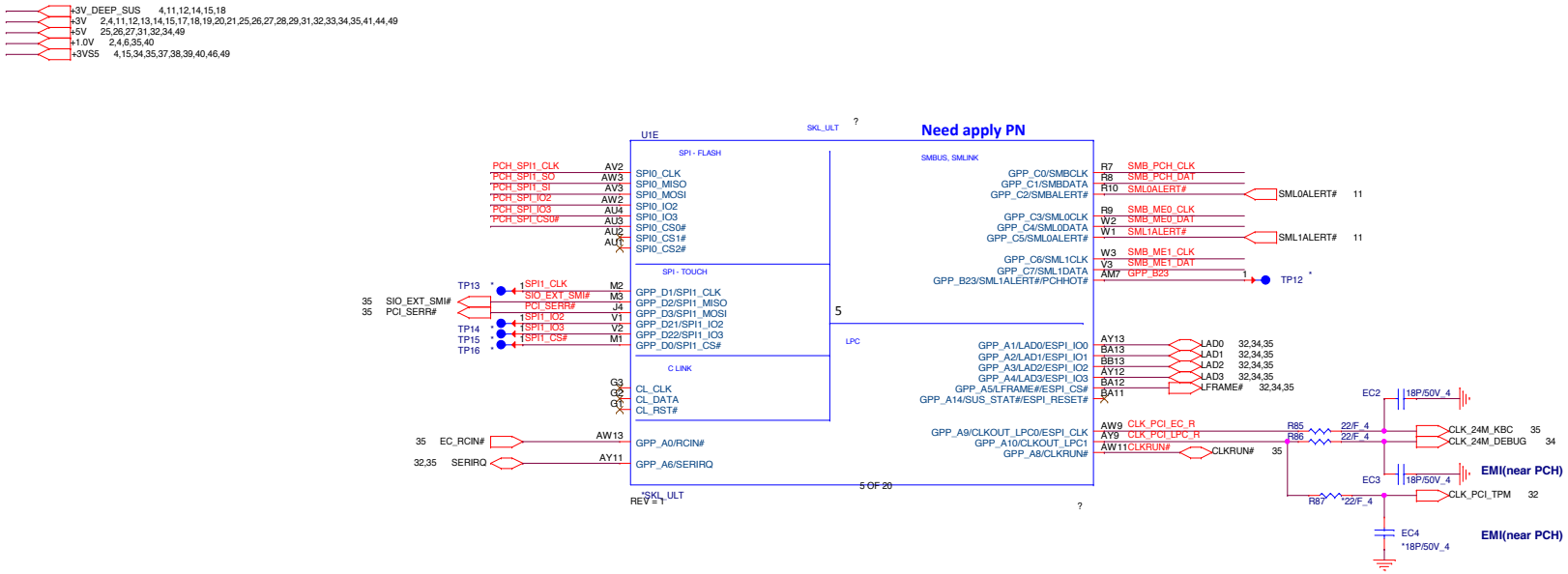
	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

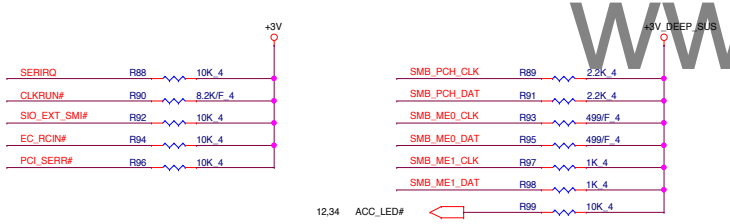
BU5

Size	Document Number	Rev
Custom	09 -- SKYLAKE 8/15 (RSV)	1A

Date: Tuesday, December 13, 2016 Sheet 9 of 49



GPIO Pull UP



PCH SPI ROM(CLG)

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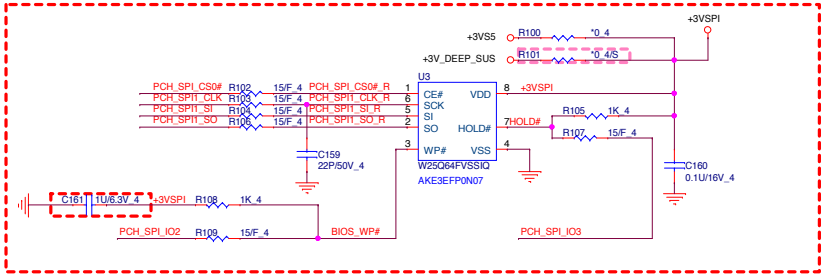
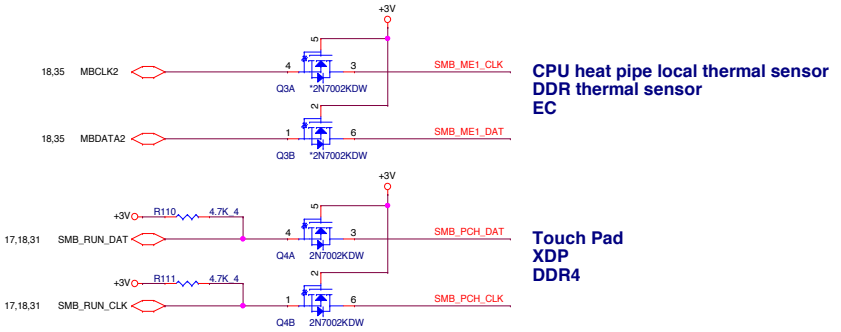
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

PCH SPI ROM(CLG)



1005 Change P/N to DFHS08FS023(Socket)

SMBus/Pull-up(CLG)



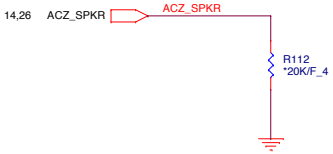
CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

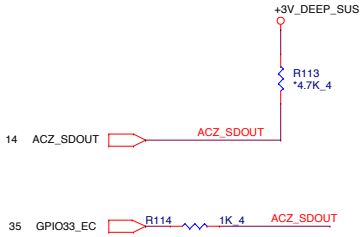
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size Custom	Document Number 10 – SKYLAKE 09/15(SPI/LPC/SM)	Rev 1A
Date: Wednesday, December 21, 2016	Sheet 10 of 49	

Functional Strap Definitions

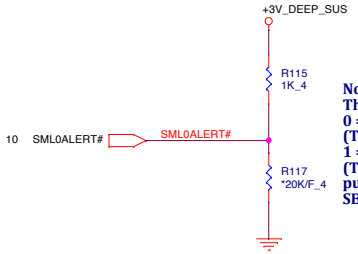
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

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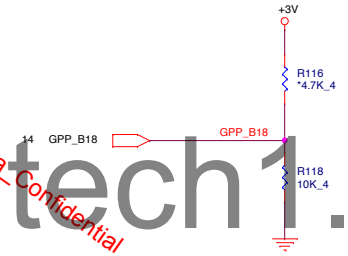
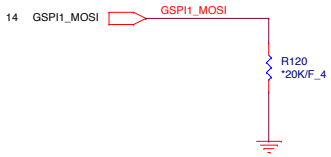
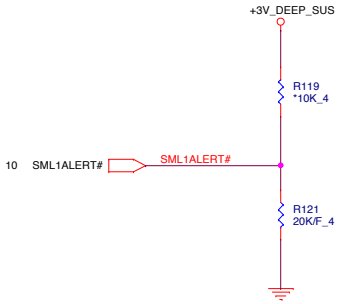


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

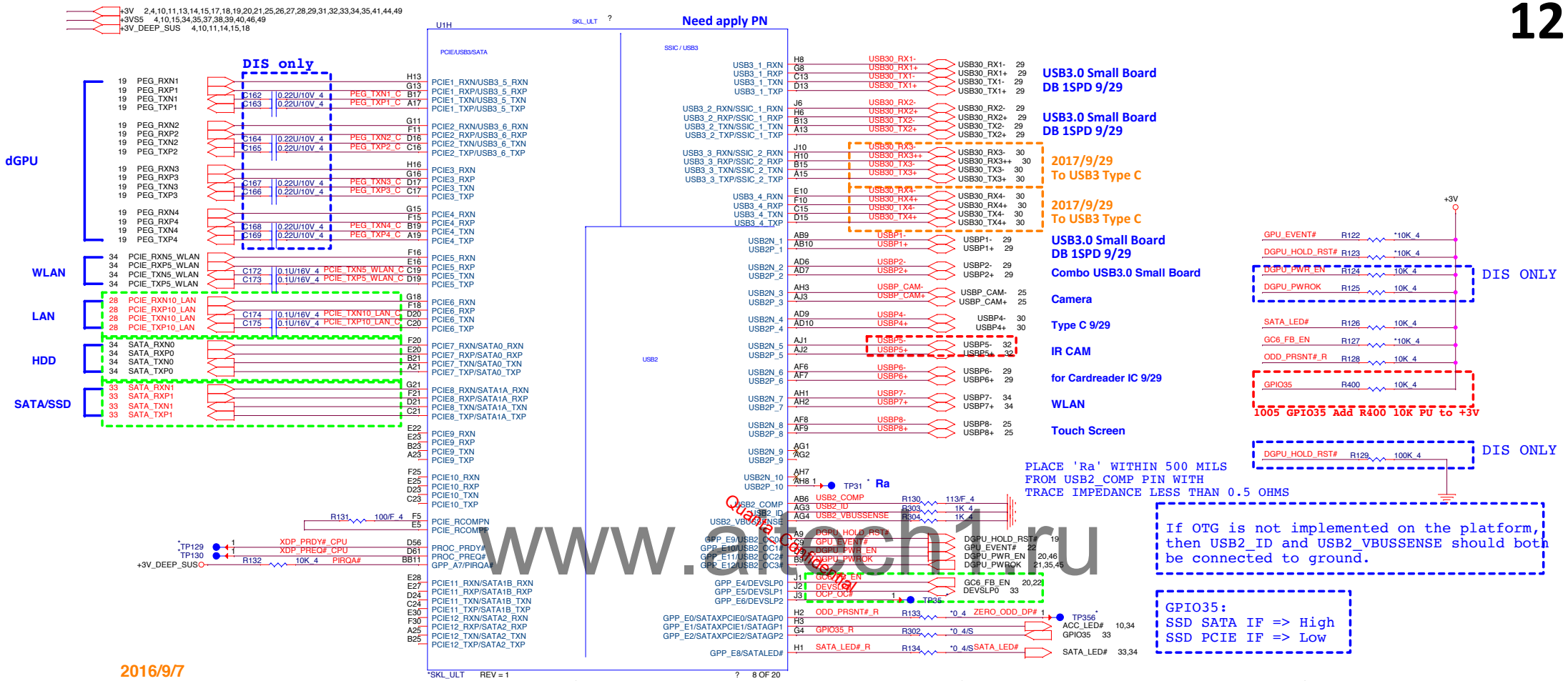


No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.



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2016/9/7
For Base-U the SATA1B/SATA2 delete

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	Un-used
Port3	dGPU	Port2	Un-used
Port4	dGPU	Port3	WLAN
Port5	WLAN	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	SATA SSD		
Port9	Un-used		
Port10	Un-used		
Port11	Un-used		
Port12	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	NC
PORT-4	NC

1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP

USB2.0 Port Mapping Table

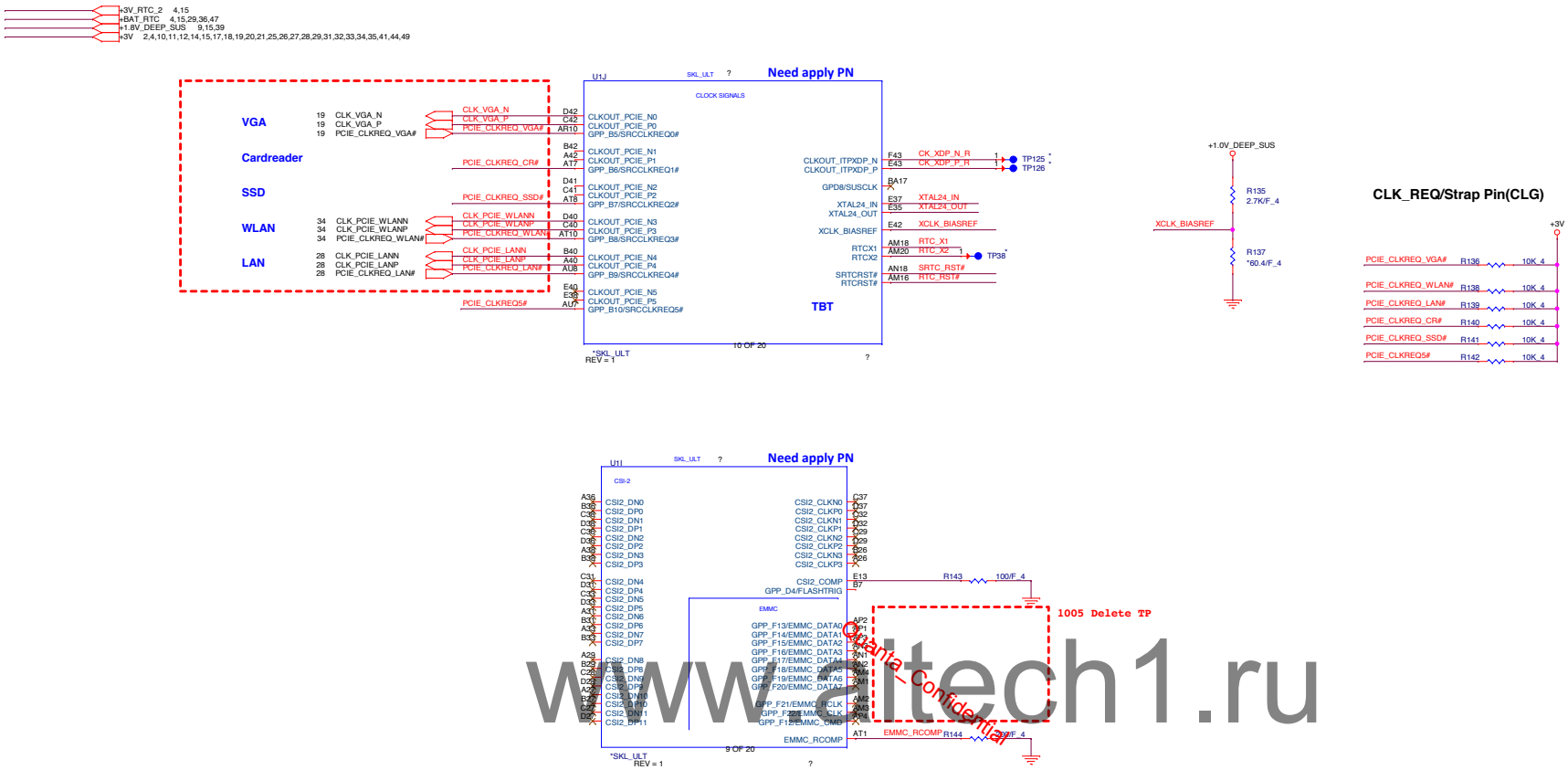
USB2.0	Function
PORT-1	USB3.0 Small Board
PORT-2	USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	Cardreader IC
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE 10/15(HDA)	1A

Date: Tuesday, December 27, 2016 Sheet 12 of 49



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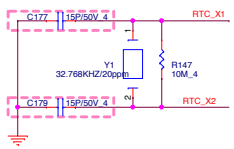
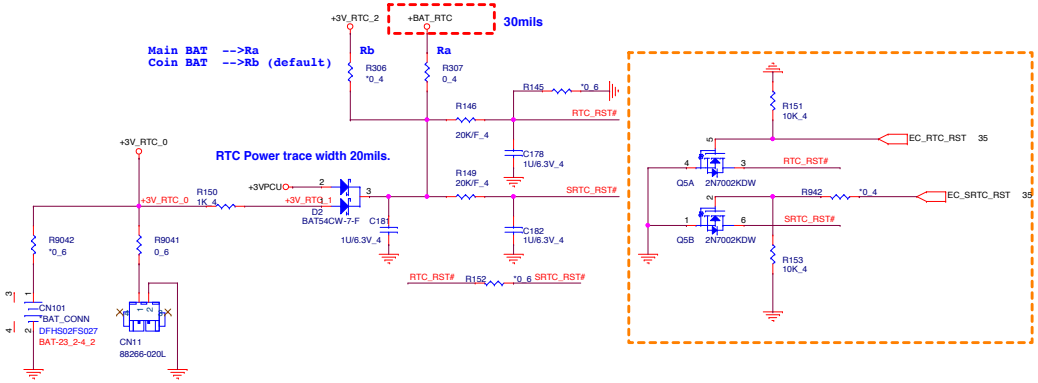
RTC Clock 32.768KHz

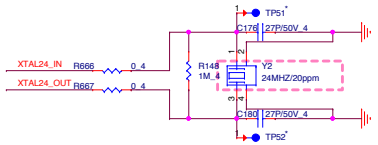


RTC Circuitry(RTC)



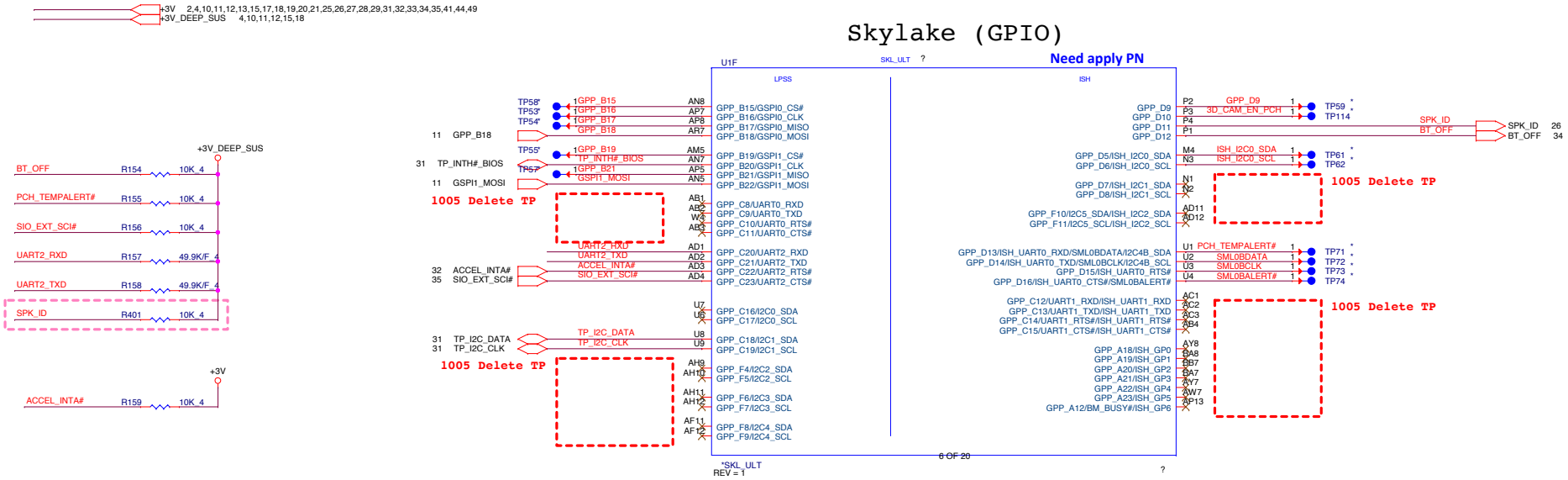
External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

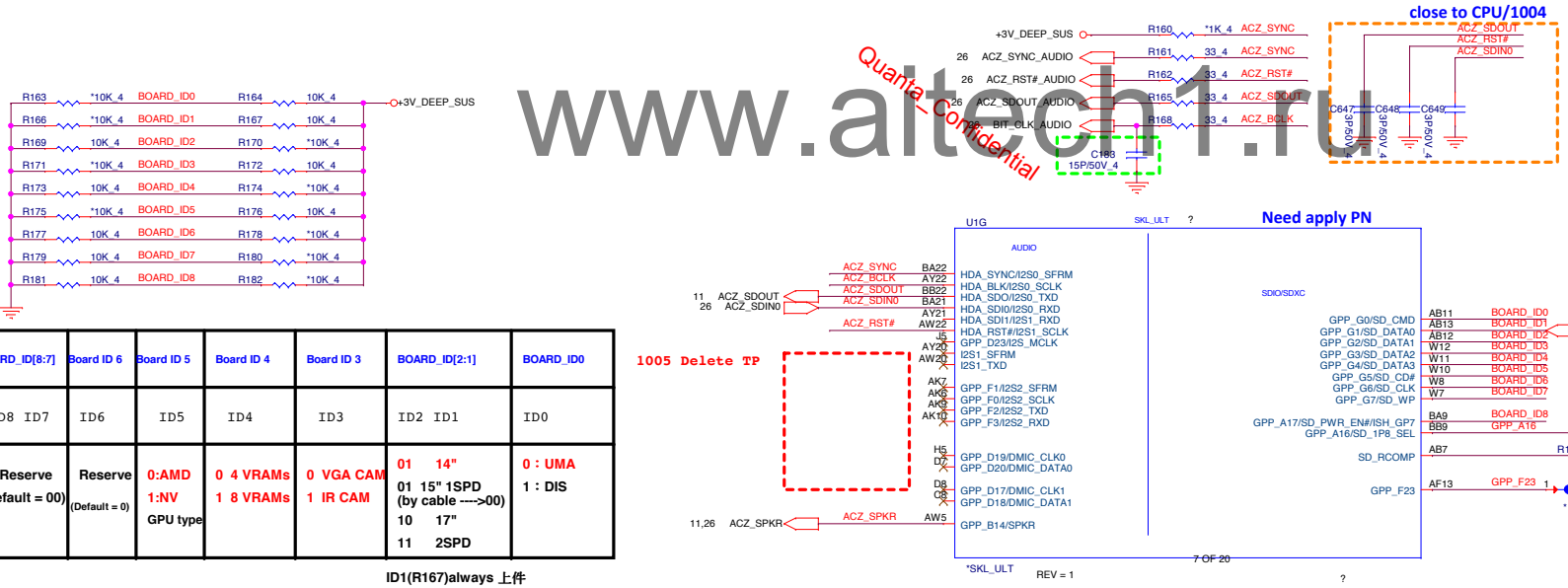


BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size Custom	Document Number 13 -- SKYLAKE 12/15 (CLK/EMMC)	Rev 1A
Date: Tuesday, December 13, 2016	Sheet 13 of 49	

Skylake (GPIO)



HDA Bus(CLG)



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Skylake U	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 0)	0:AMD 1:NV GPU type	0 4 VRAMs 1 8 VRAMs	0 VGA CAM 1 IR CAM	01 14" 01 15" 1SPD (by cable ---->00) 10 17" 11 2SPD	0 : UMA 1 : DIS

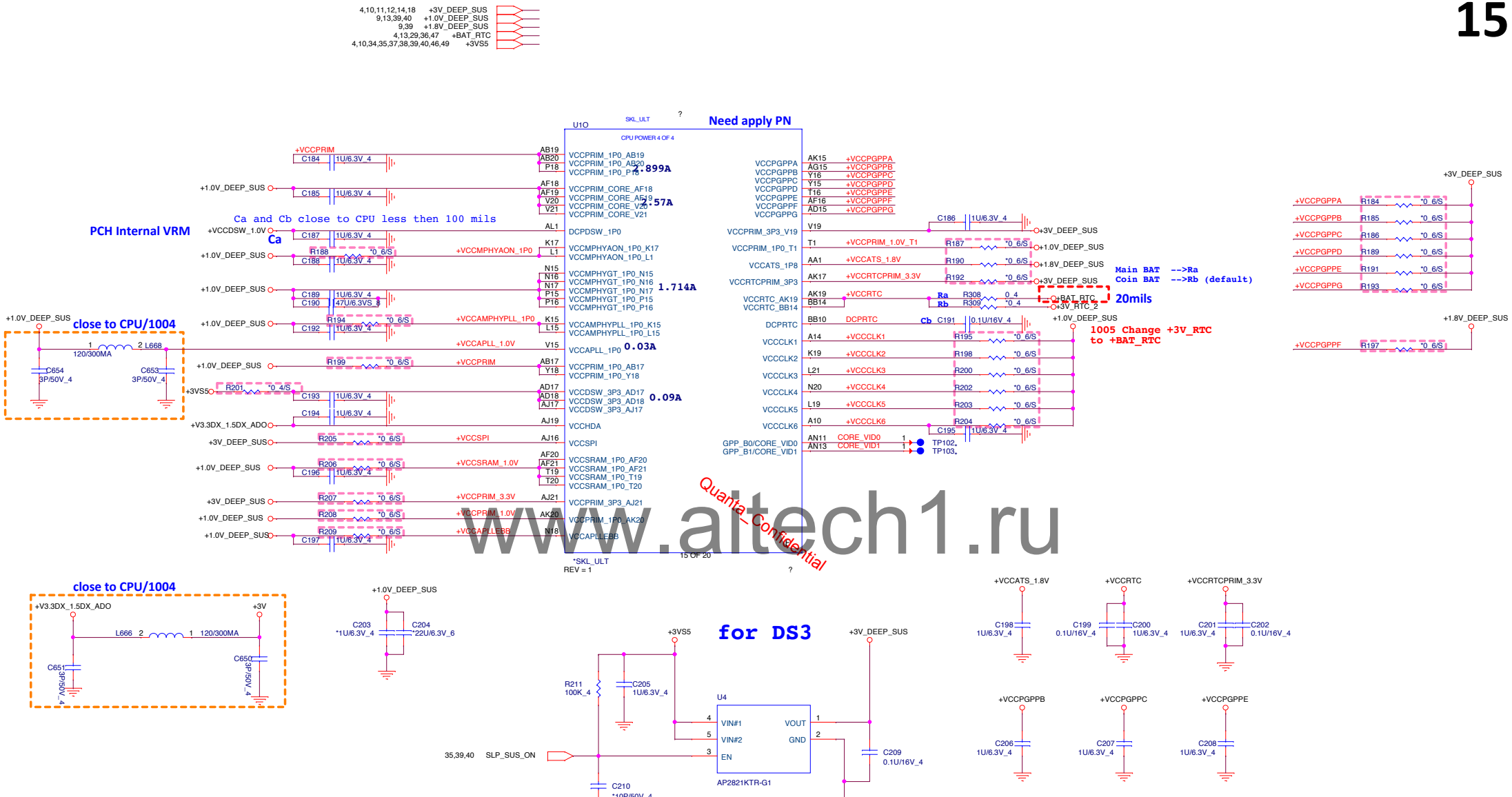
ID1(R167)always 上件

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

BU5

Size	Document Number	Rev
Custom	14 – SKYLAKE 13/15 (GPIO)	1A

Date: Tuesday, December 27, 2016 Sheet 14 of 49



PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	15 -- SKYLAKE 14/15(PCH POWER)	1A

Date: Tuesday, December 13, 2016 Sheet 15 of 49

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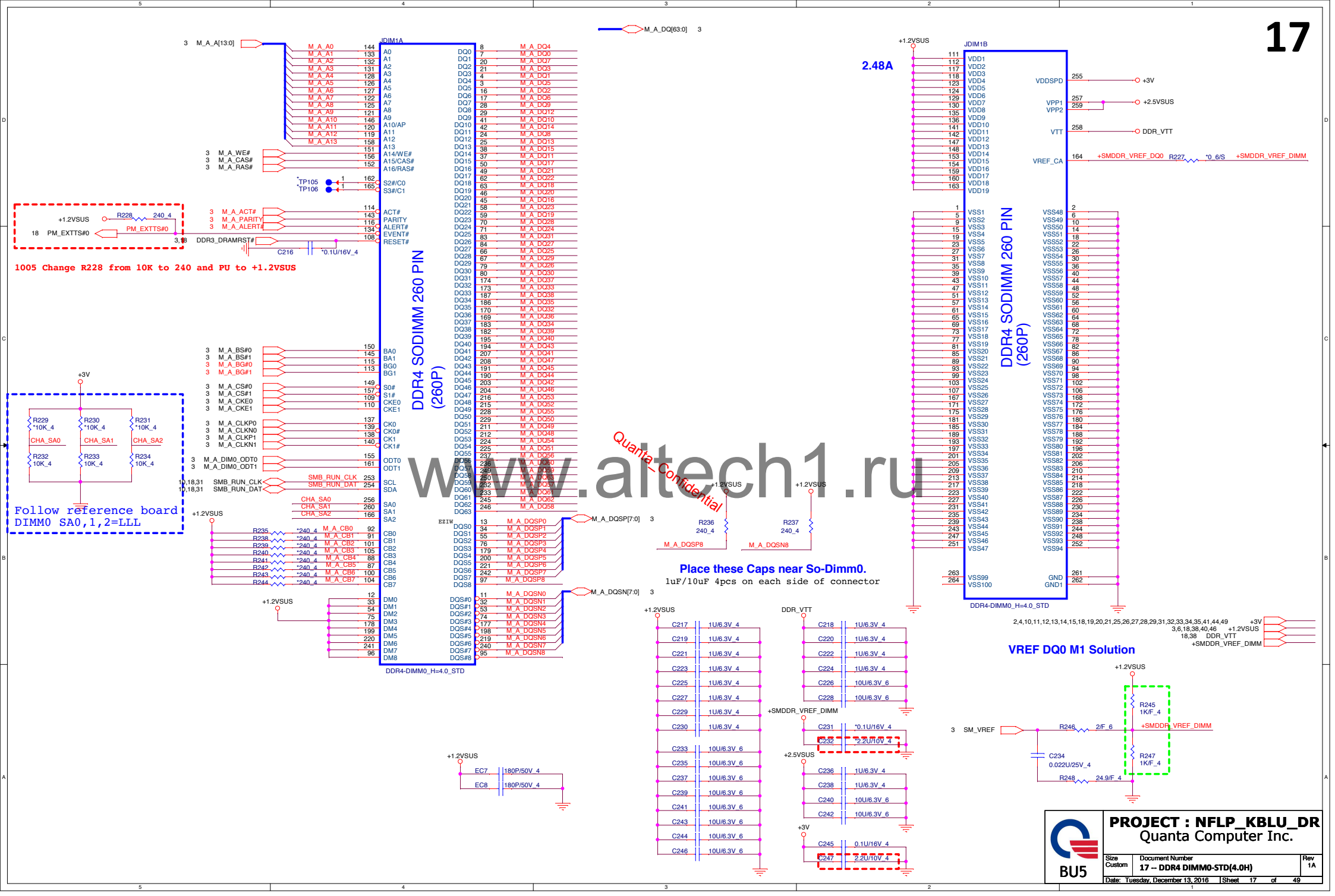
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
	16 -- SKYLAKE 15/15 XDP&APS *	1A

Date: Tuesday, December 13, 2016 | Sheet 16 of 49


JDIM1A
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
2.48A
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
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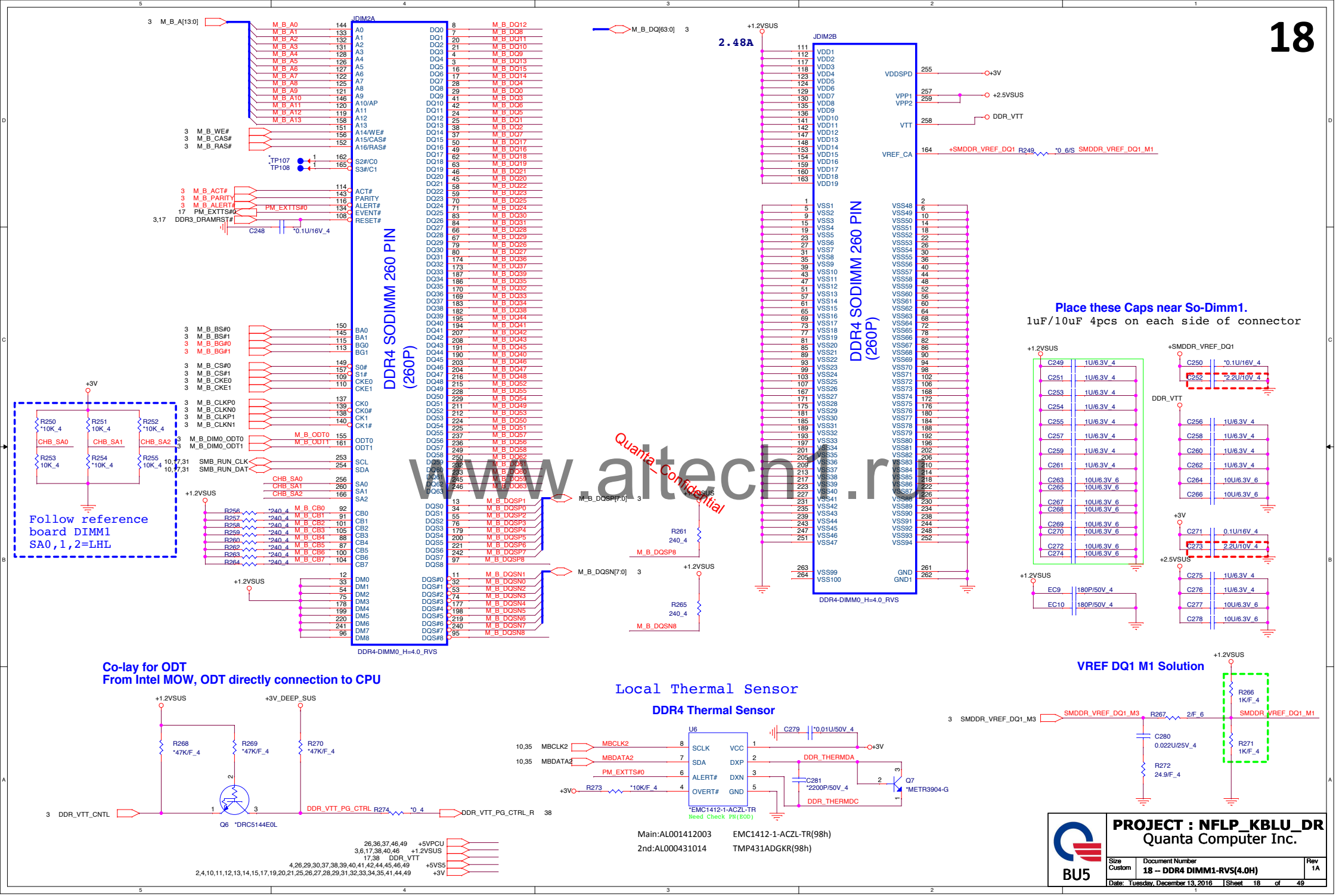
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
Date: Tuesday, December 13, 2016
Sheet 17 of 49



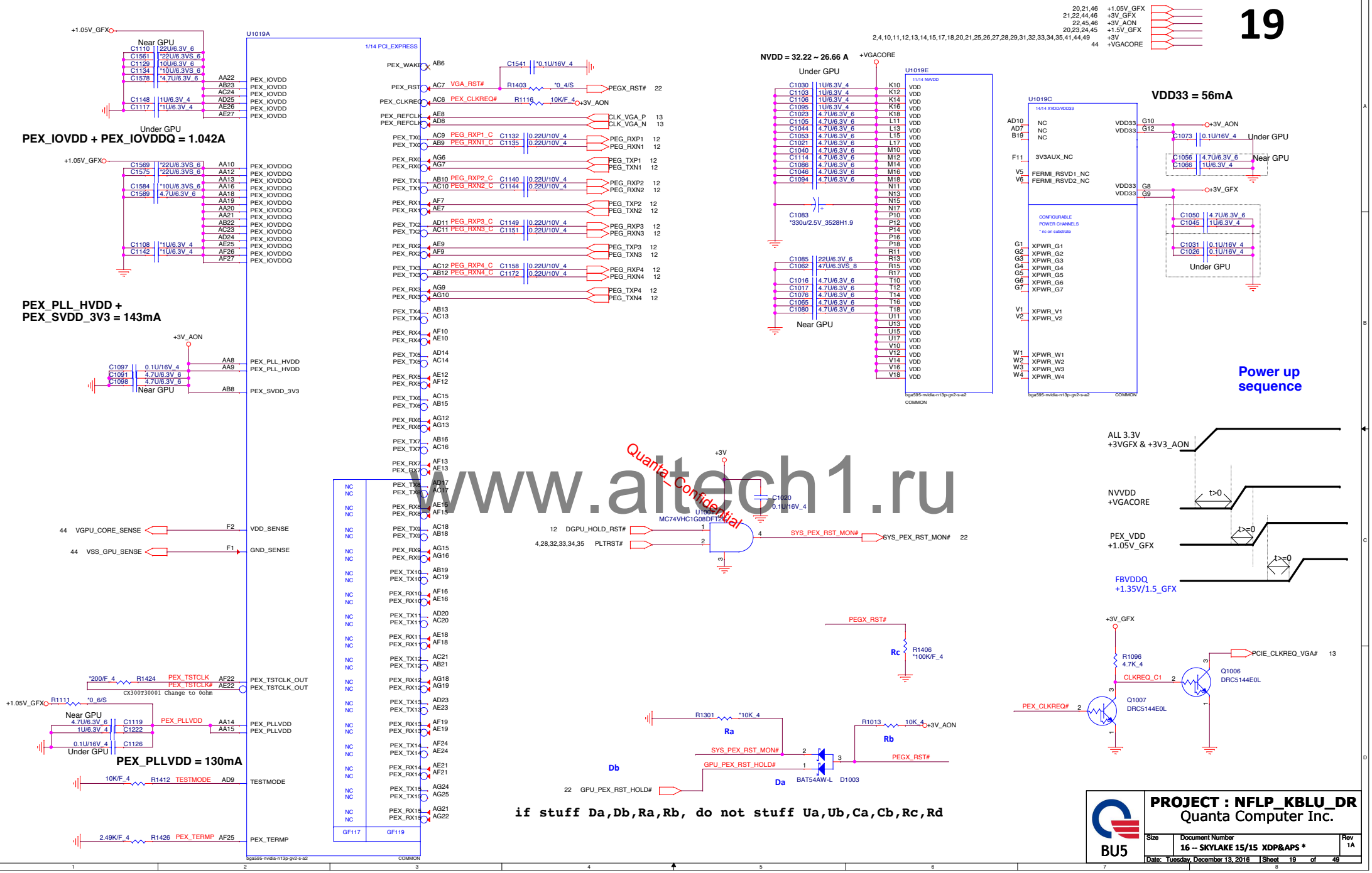
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

26,36,37,46,49	+5VPCU
3,6,17,38,40,46	+1.2VSUS
17,38	DDR_VTT
4,26,29,30,37,38,39,40,41,42,44,45,46,49	+5VS5
2,4,10,11,12,13,14,15,17,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44,49	+3V

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	18 -- DDR4 DIMM1-RVS(4.0H)	1A

Date: Tuesday, December 13, 2016 Sheet 18 of 49



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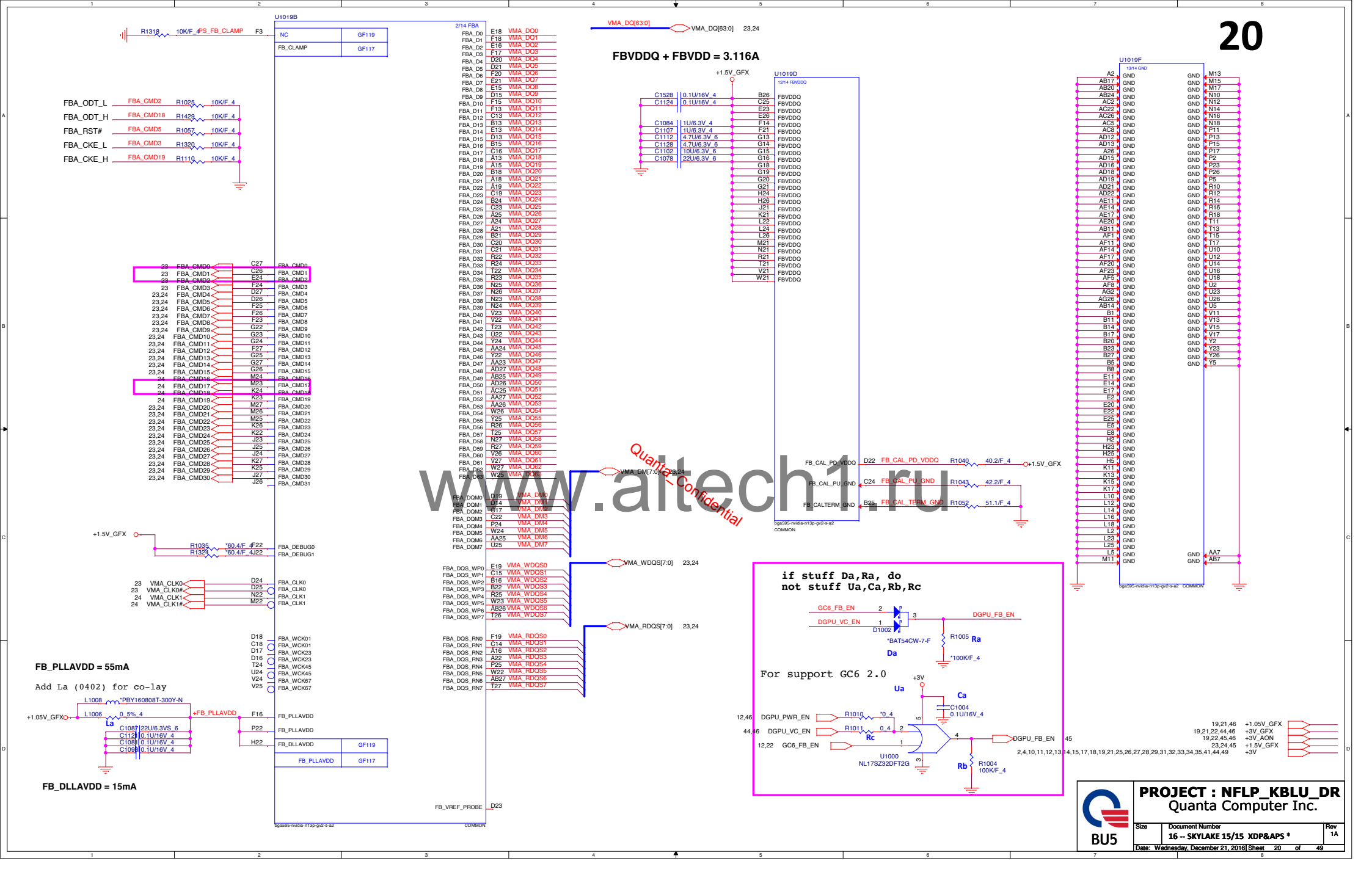
U1019B
2/14 FBA
R1318 10K/F_4 PS_FB_CLAMP F3
NC GF119
FB_CLAMP GF117
FBA_ODT_L FBA_CMD2 R1025 10K/F_4
FBA_ODT_H FBA_CMD18 R1429 10K/F_4
FBA_RST# FBA_CMD5 R1057 10K/F_4
FBA_CKE_L FBA_CMD3 R1320 10K/F_4
FBA_CKE_H FBA_CMD19 R1110 10K/F_4
VMA_DQ[63:0]
VMA_DQ[63:0] 23,24
FBVDDQ + FBVDD = 3.116A
+1.5V_GFX
U1019D
12/14 FBVDDQ
C1528 0.1U/16V_4
C1124 0.1U/16V_4
C1084 1U/6.3V_4
C1107 1U/6.3V_4
C1112 4.7U/6.3V_6
C1128 4.7U/6.3V_6
C1102 10U/6.3V_6
C1078 22U/6.3V_6
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1040 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1043 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R1052 51.1/F_4
bga595-nvidia-n13p-gv2-s-a2 COMMON
U1019F
13/14 GND
bga595-nvidia-n13p-gv2-s-a2 COMMON
+1.5V_GFX
R1035 *60.4/F_4 F22 FBA_DEBUG0
R1324 *60.4/F_4 J22 FBA_DEBUG1
23 VMA_CLK0 D24 FBA_CLK0
23 VMA_CLK0# D25 FBA_CLK0
24 VMA_CLK1 N22 FBA_CLK1
24 VMA_CLK1# M22 FBA_CLK1
D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67
FB_PLLAVDD = 55mA
Add La (0402) for co-lay
L1008 *PBY160808T-300Y-N
+1.05V_GFX L1006 0_5%_4 +FB_PLLAVDD
La
C1087 22U/6.3VS_6
C1121 0.1U/16V_4
C1088 0.1U/16V_4
C1089 0.1U/16V_4
F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22 FB_DLLAVDD
FB_DLLAVDD GF119
FB_PLLAVDD GF117
FB_DLLAVDD = 15mA
FB_VREF_PROBE D23
bga595-nvidia-n13p-gv2-s-a2 COMMON
VMA_DM[7:0] 23,24
VMA_WDQS[7:0] 23,24
VMA_RDQS[7:0] 23,24
if stuff Da,Ra, do
not stuff Ua,Ca,Rb,Rc
GC6_FB_EN
DGPU_VC_EN
D1002 *BAT54CW-7-F
Da
R1005 Ra *100K/F_4
DGPU_FB_EN
For support GC6 2.0
+3V
Ua
Ca
C1004 0.1U/16V_4
12,46 DGPU_PWR_EN R1010 *0_4
44,46 DGPU_VC_EN R1011 0_4
Rc
12,22 GC6_FB_EN
U1000 NL17SZ32DFT2G
Rb R1004 100K/F_4
DGPU_FB_EN 45
19,21,46 +1.05V_GFX
19,21,22,44,46 +3V_GFX
19,22,45,46 +3V_AON
23,24,45 +1.5V_GFX
+3V
2,4,10,11,12,13,14,15,17,18,19,21,25,26,27,28,29,31,32,33,34,35,41,44,49
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BU5
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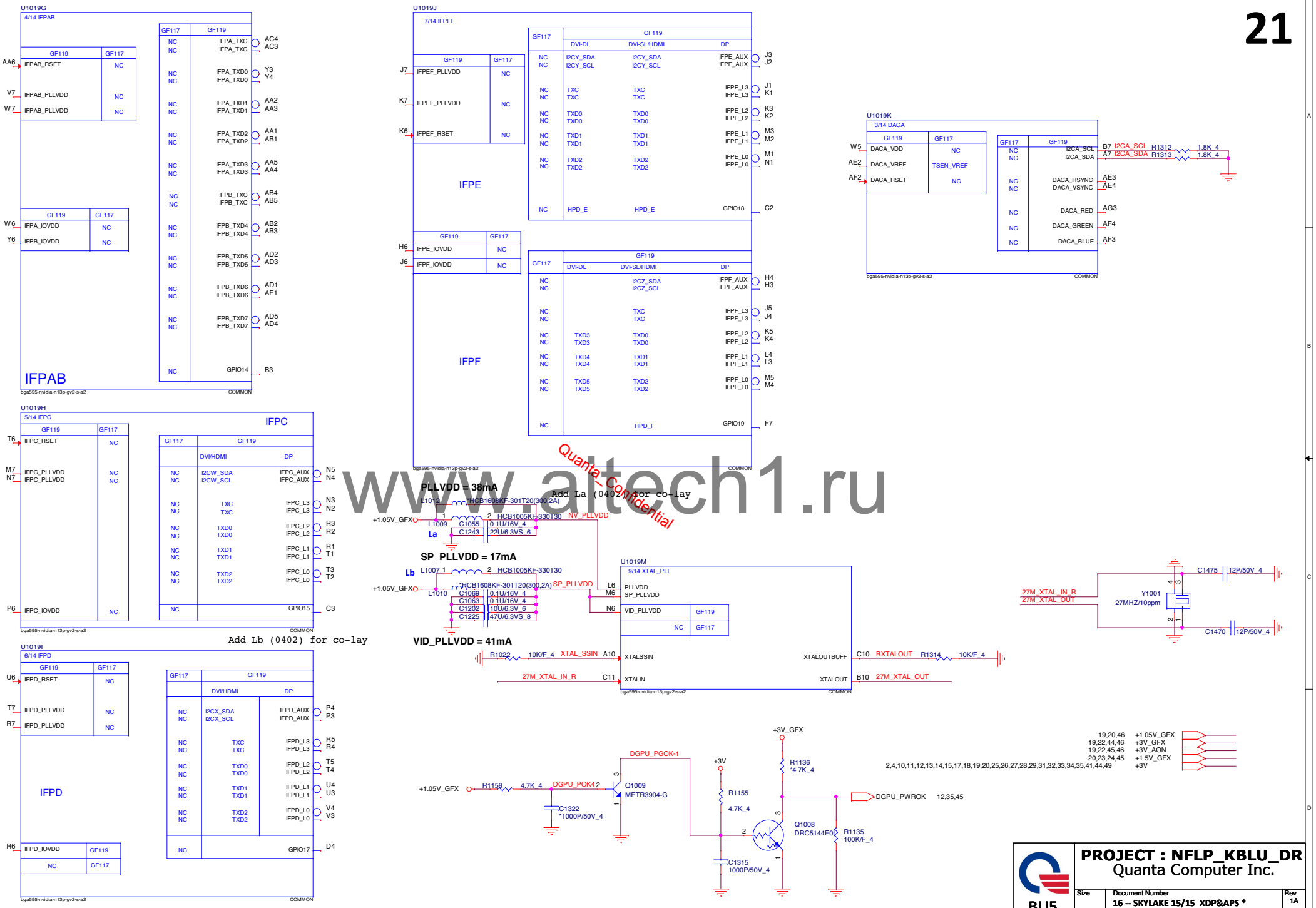
Quanta Computer Inc.
Size
Document Number
16 – SKYLAKE 15/15 XDP&APS *
Rev 1A
Date: Wednesday, December 21, 2016 Sheet 20 of 49



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	16 -- SKYLAKE 15/15 XDP&APS *	1A

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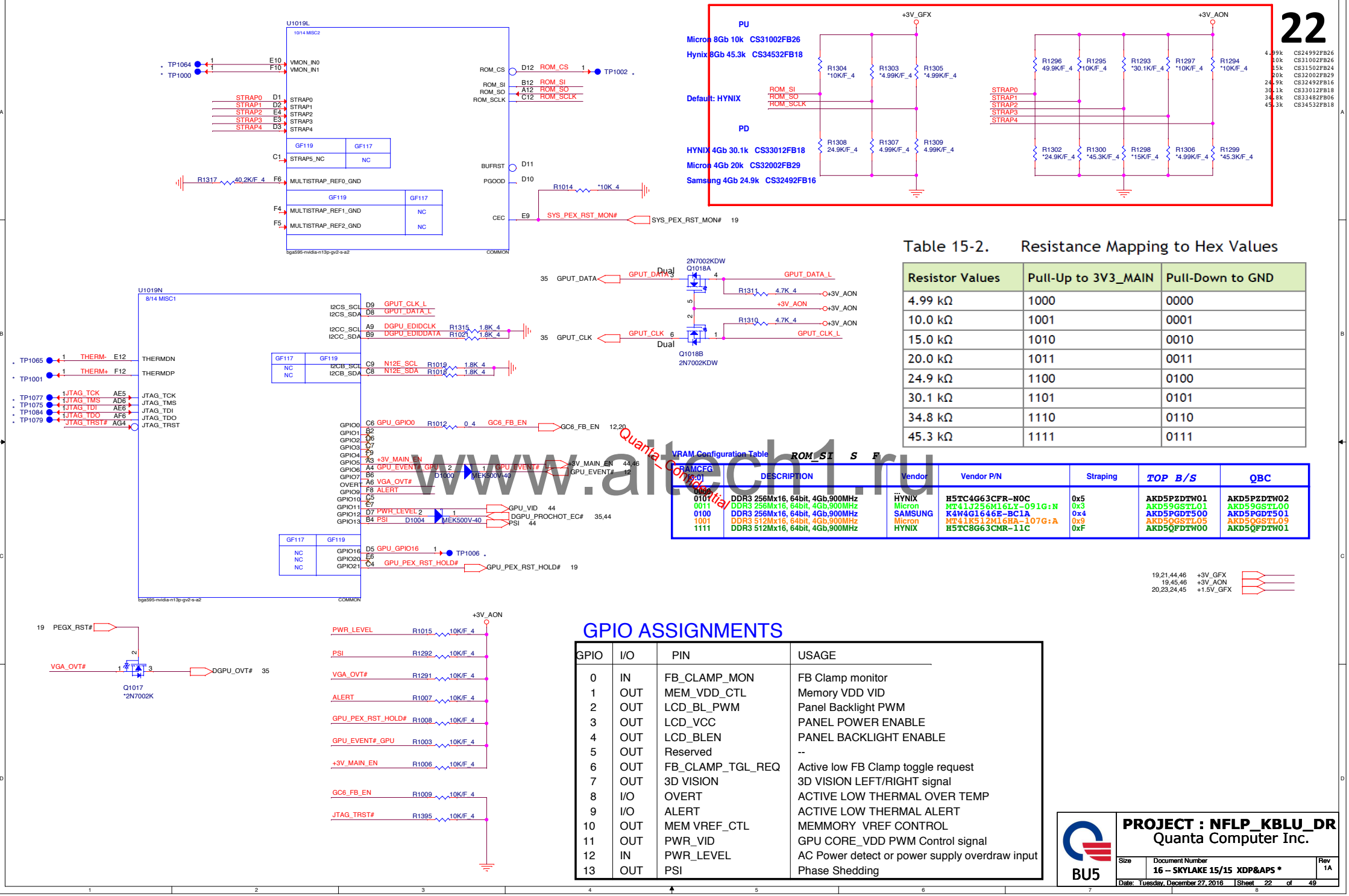

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0000	...	...				
0101	DDR3 256Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC4G63CFR-NOC	0x5	AKD5PZDTW01	AKD5PZDTW02
0011	DDR3 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501
1001	DDR3 512Mx16, 64bit, 4Gb,900MHz	Micron	MT41K512M16HA-107G:A	0x9	AKD5QGSTL05	AKD5QGSTL09
1111	DDR3 512Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC8G63CMR-11C	0xF	AKD5QFDTW00	AKD5QFDTW01

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

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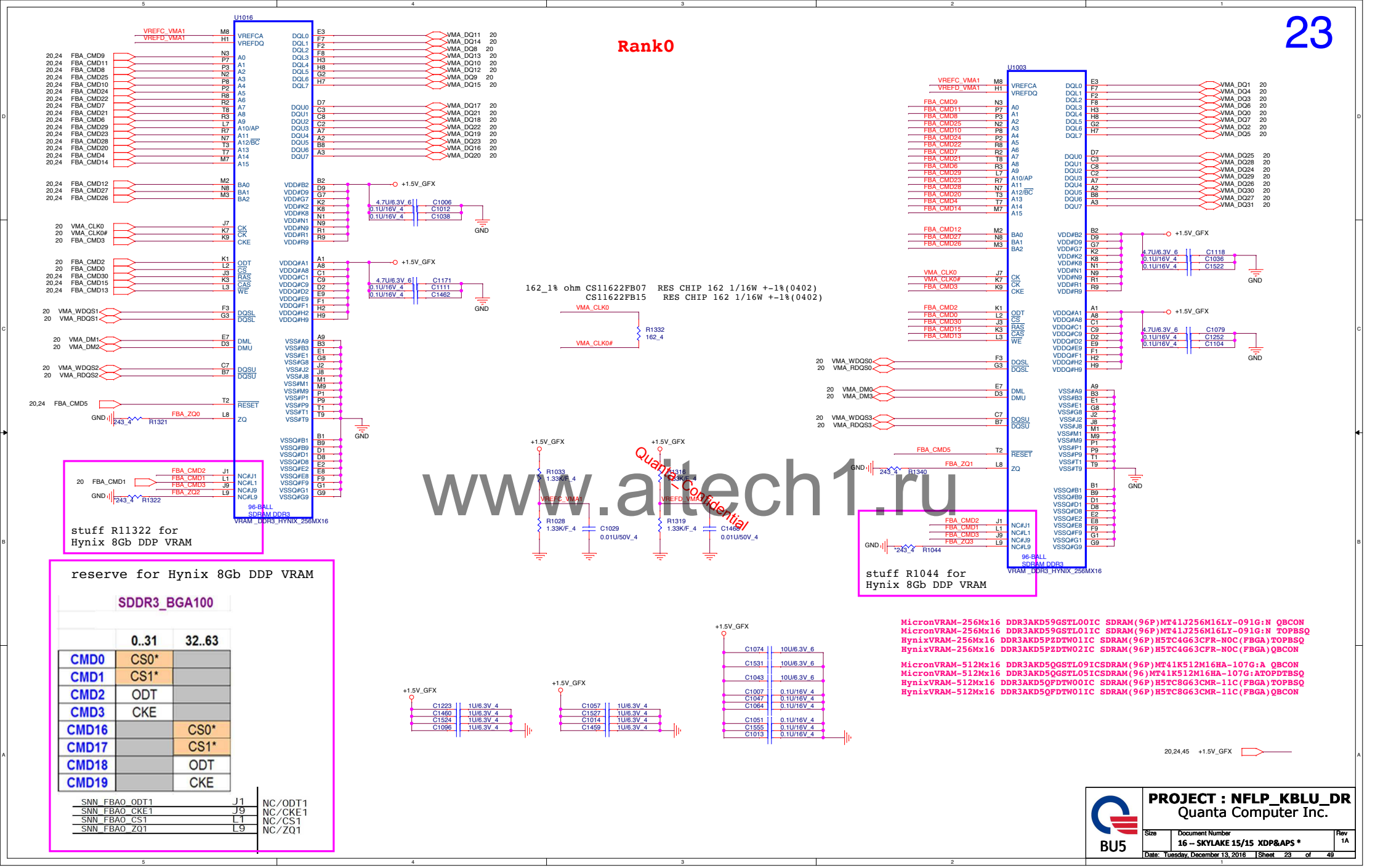

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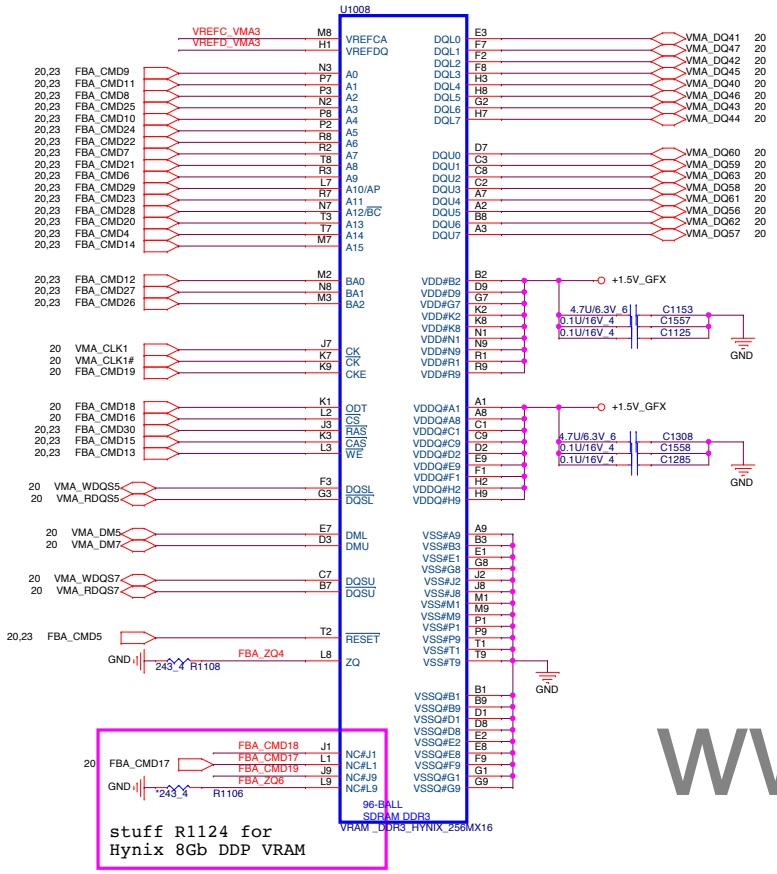
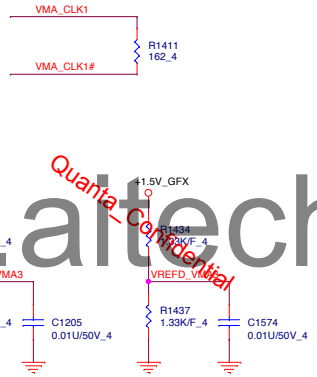
Rank0

1114SWAP

1114SWAP



162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)



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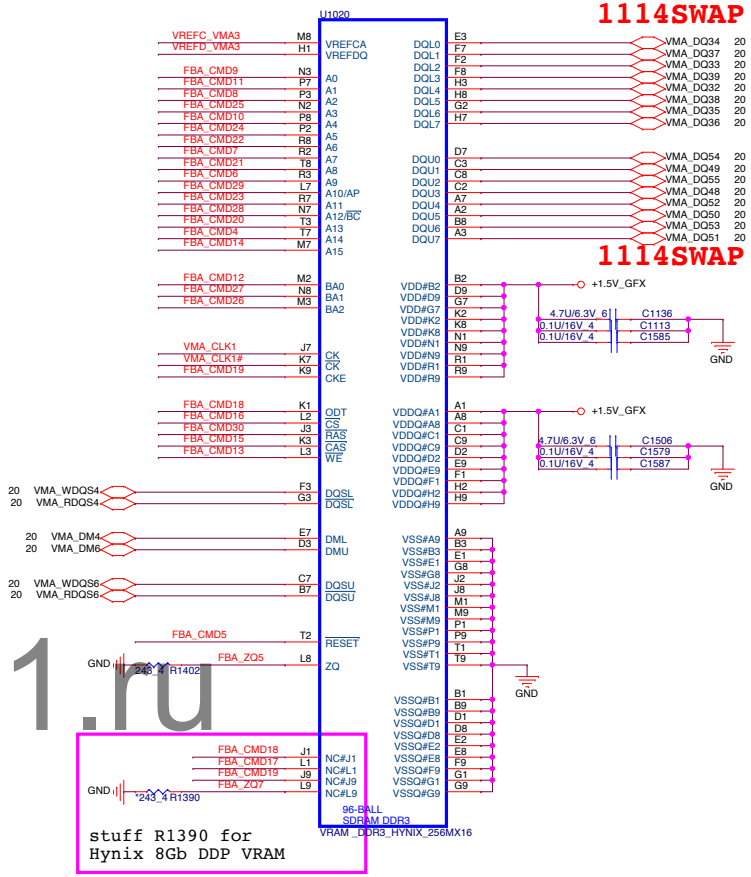
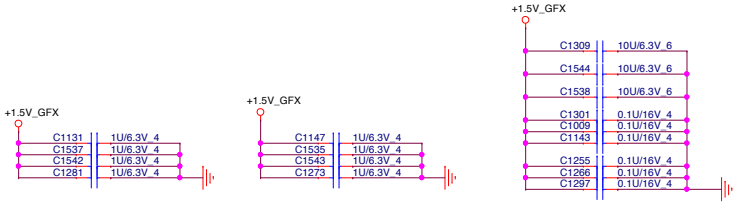
1114SWAP

1114SWAP



MicronVRAM-256Mx16 DDR3AKD59GSTL00IC SDRAM(96P)MT41J256M16LY-091G:N QBCON
MicronVRAM-256Mx16 DDR3AKD59GSTL01IC SDRAM(96P)MT41J256M16LY-091G:N TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW01IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW02IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)QBCON

MicronVRAM-512Mx16 DDR3AKD5QGSTL09ICSDRAM(96P)MT41K512M16HA-107G:A QBCON
MicronVRAM-512Mx16 DDR3AKD5QGSTL05ICSDRAM(96)MT41K512M16HA-107G:ATOPDTBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW00IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)TOPBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW01IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)QBCON



20,23,45 +1.5V_GFX

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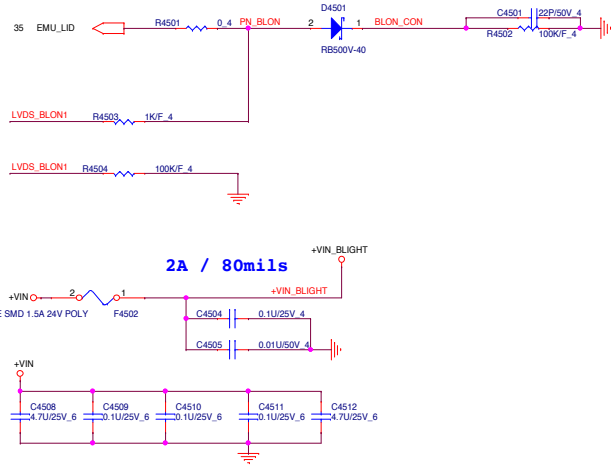
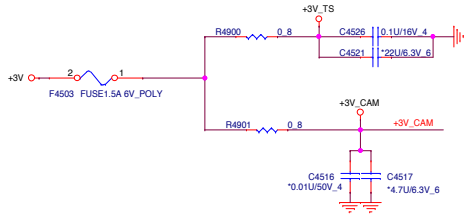
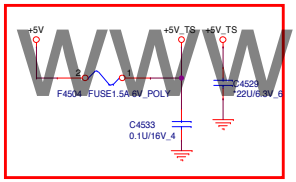
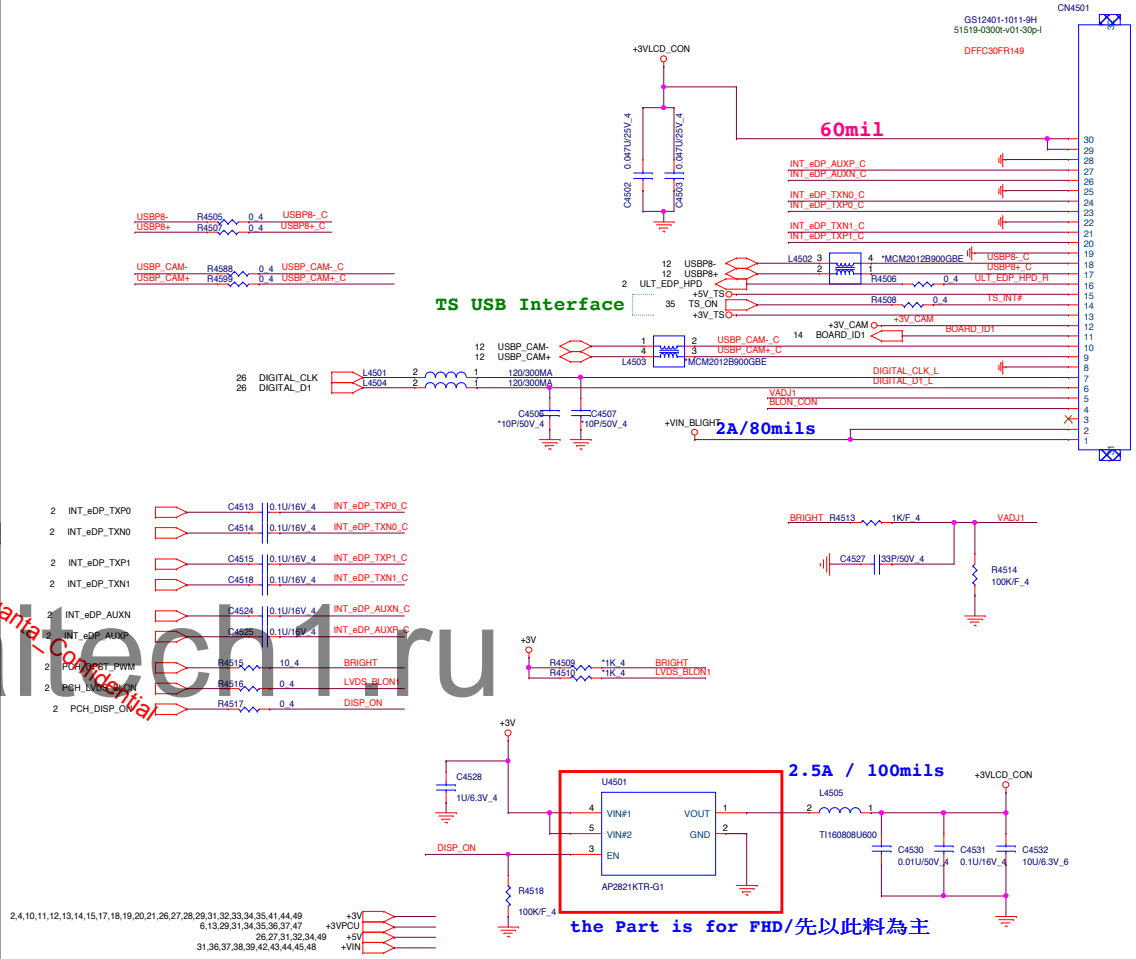
LID Switch







eDP Conn.



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Size: Custom	Document Number: 27 -- eDP CONN/LID/CAM/D-MIC/TS	Rev: 1A
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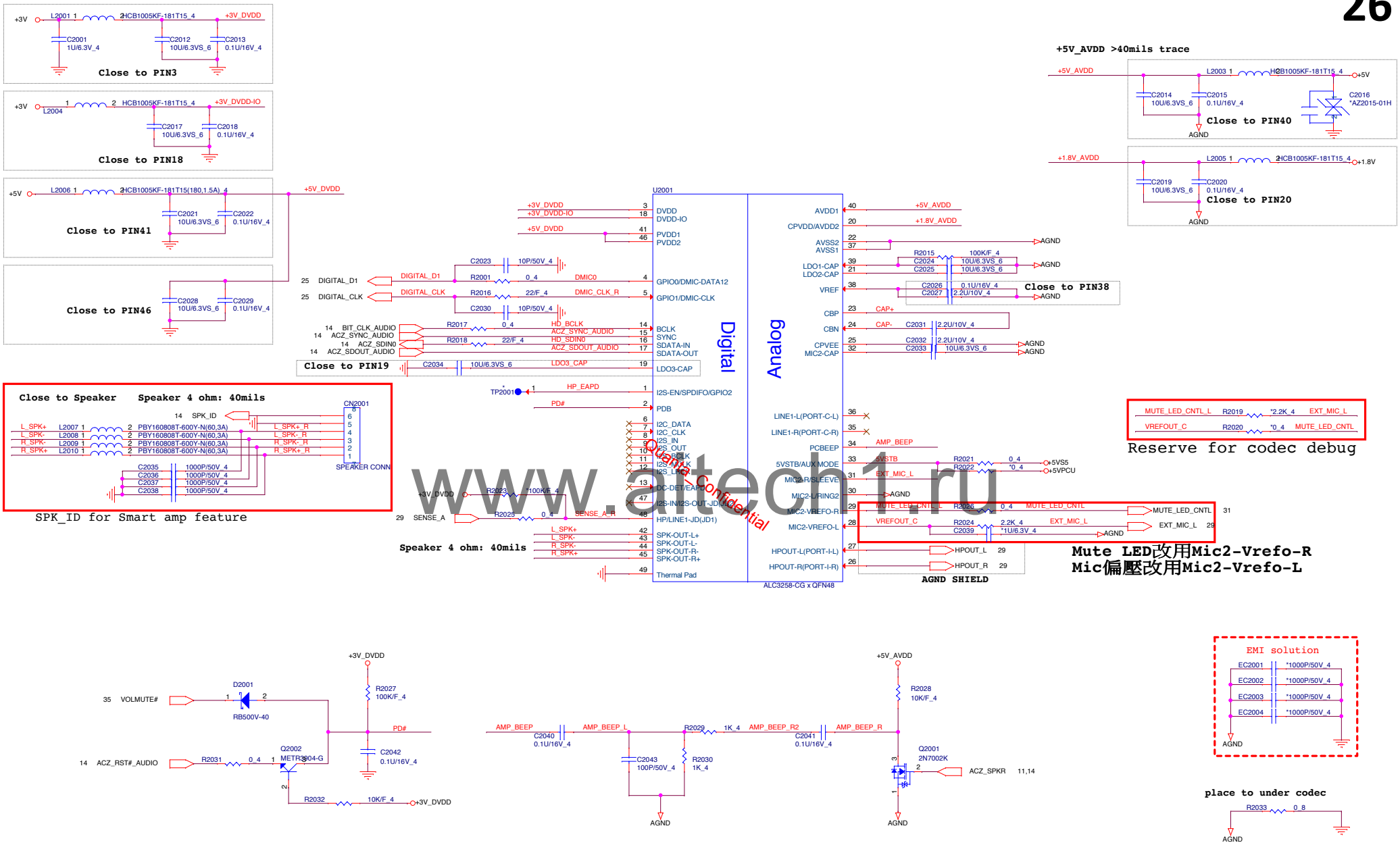

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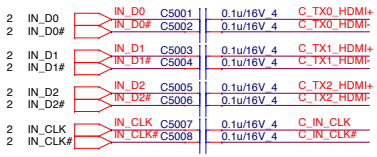
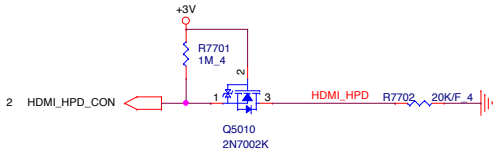
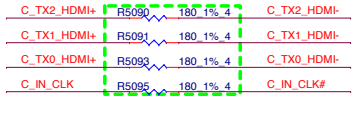
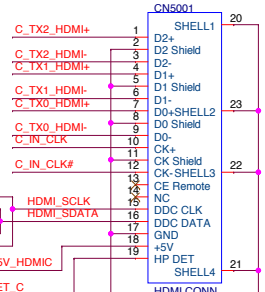
HDMI CONN

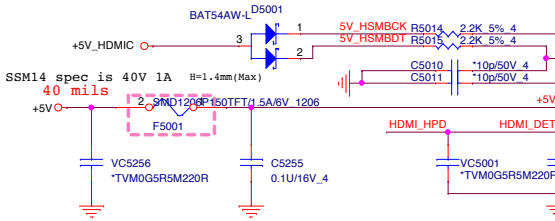




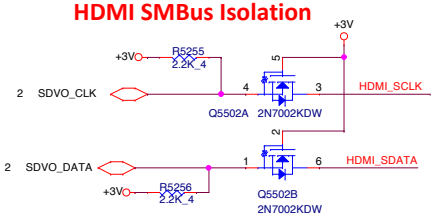
EMI Solution



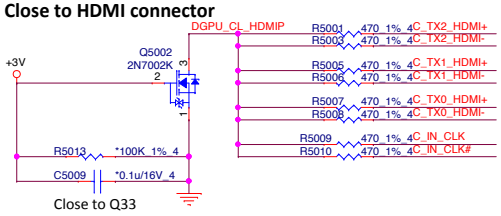




HDMI SMBus Isolation



Close to HDMI connector



Head Phone out

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BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
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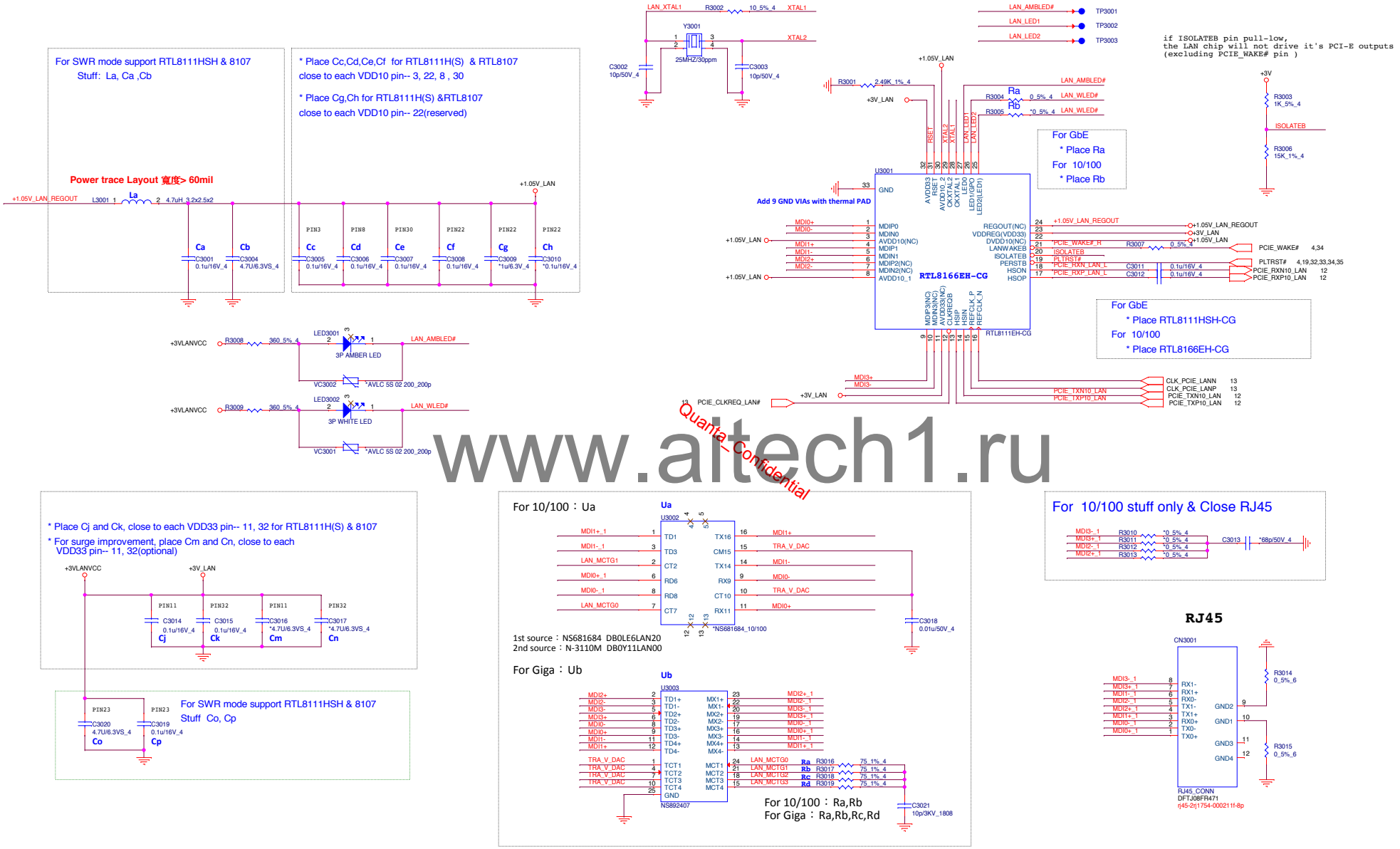
LAN RTL8107EH/RTL8111HSH



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For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.		
	Size C	Document Number 30 – LAN RTL8107EH/RTL8111HSH	Rev 1A
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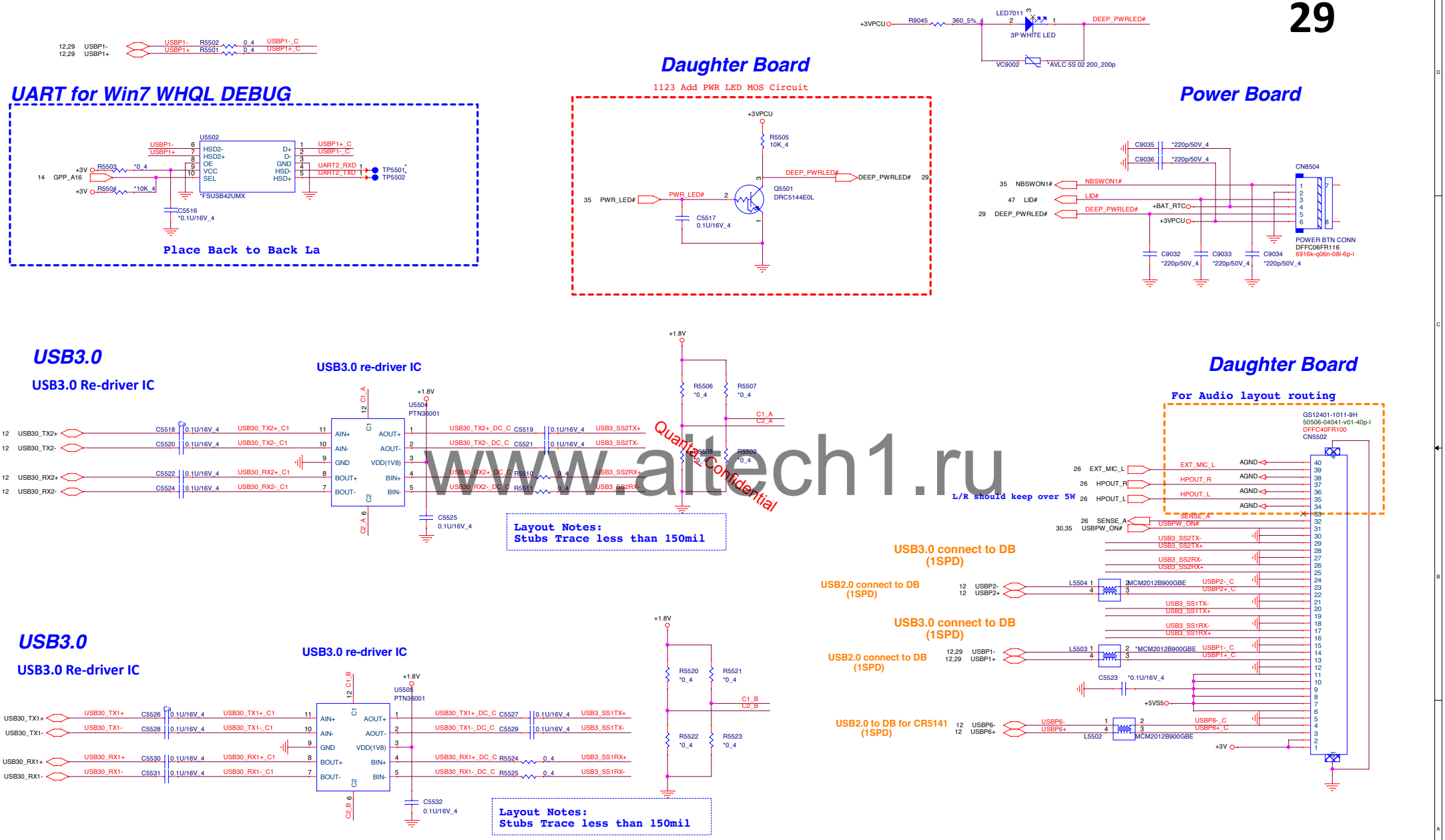

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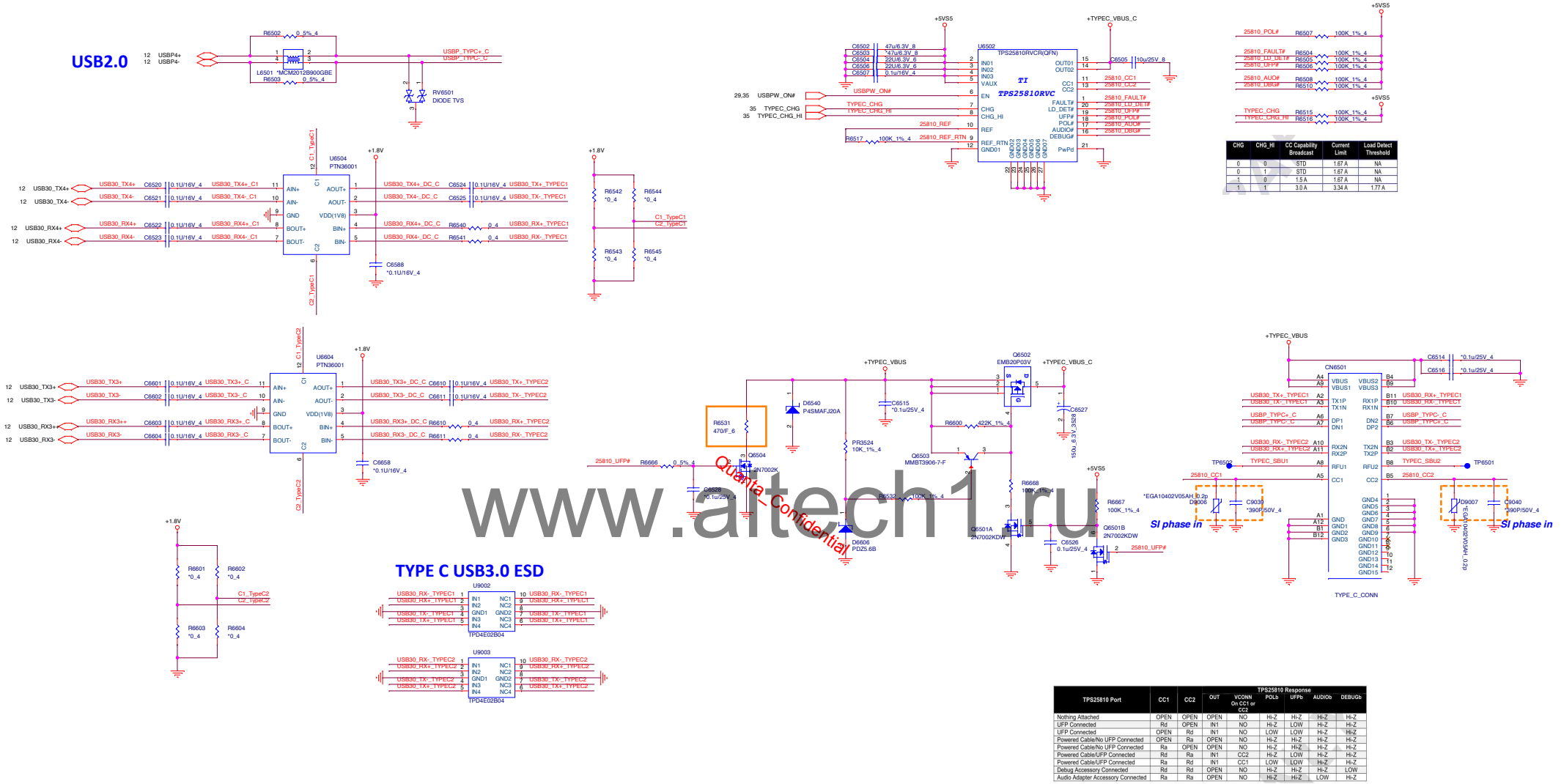
USB TYPE-C - TPS25810



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	TPS25810 Response POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

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Size: Custom | Document Number: 32 -- USB SW & TYPE-C -TPS25810 | Rev: 1A

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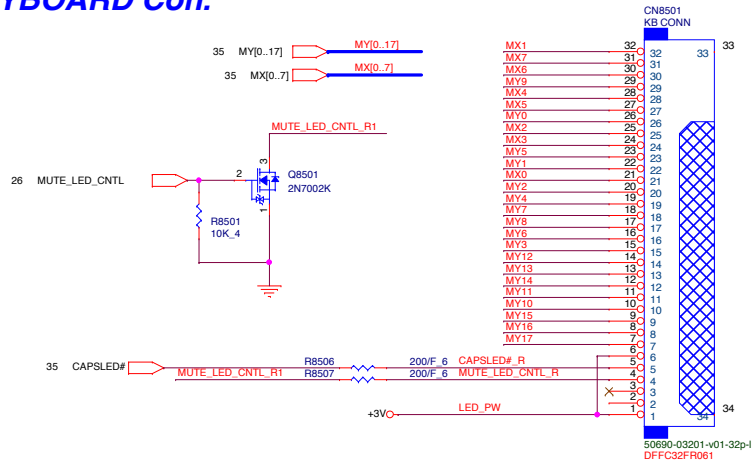
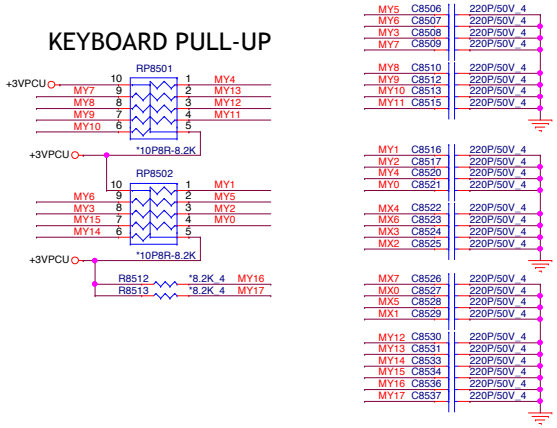
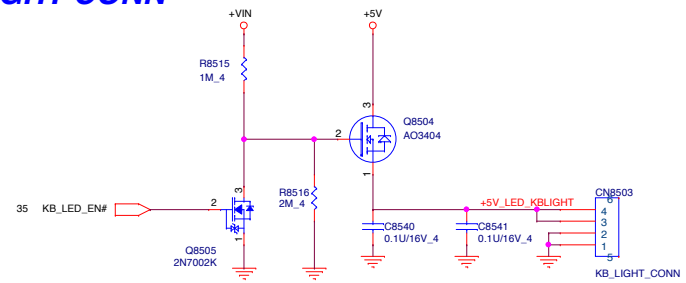
KEYBOARD Con.



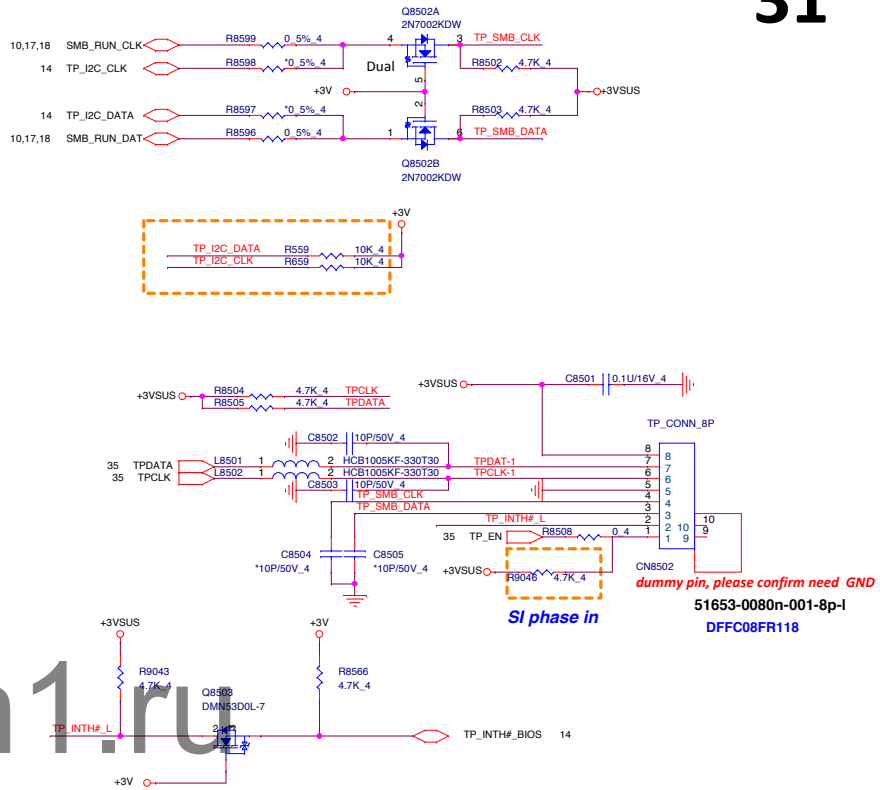
KEYBOARD PULL-UP



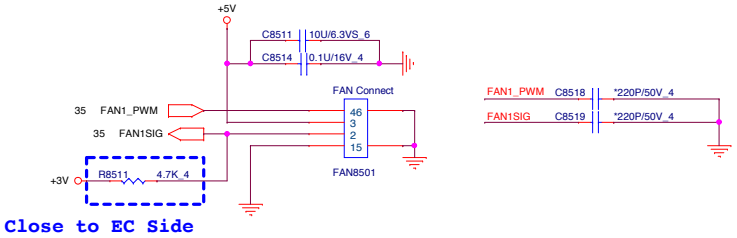
KB LIGHT CONN



Touch Pad Connector



FAN



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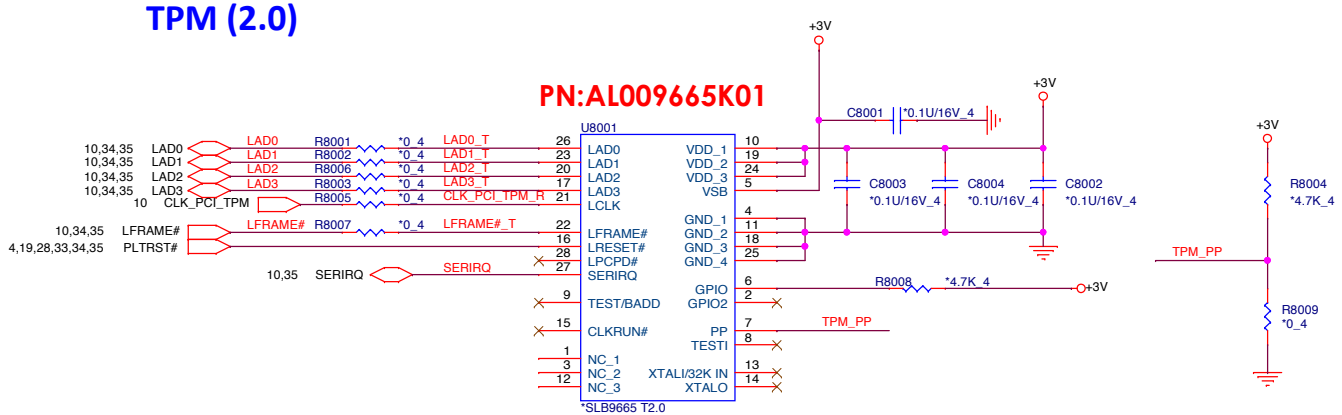
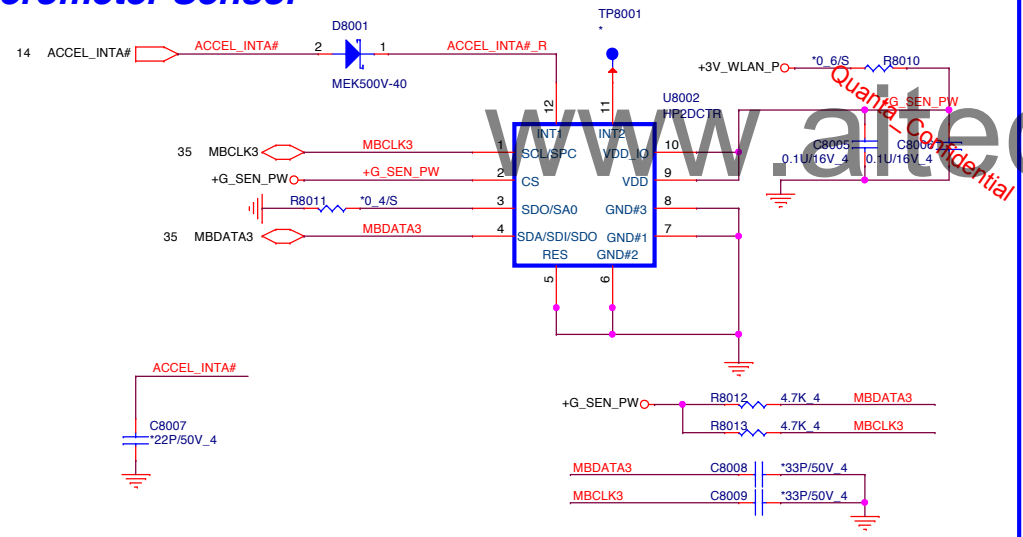
TPM (2.0)

PN:AL009665K01

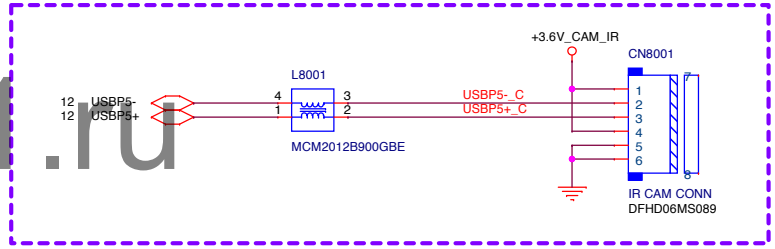


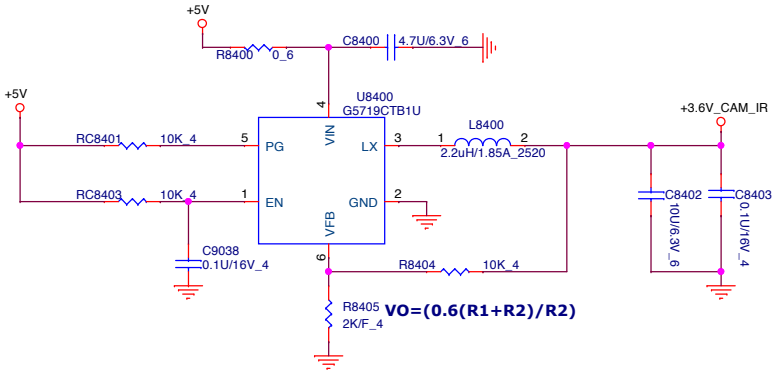
Accelerometer Sensor



IR CAM

current:4A





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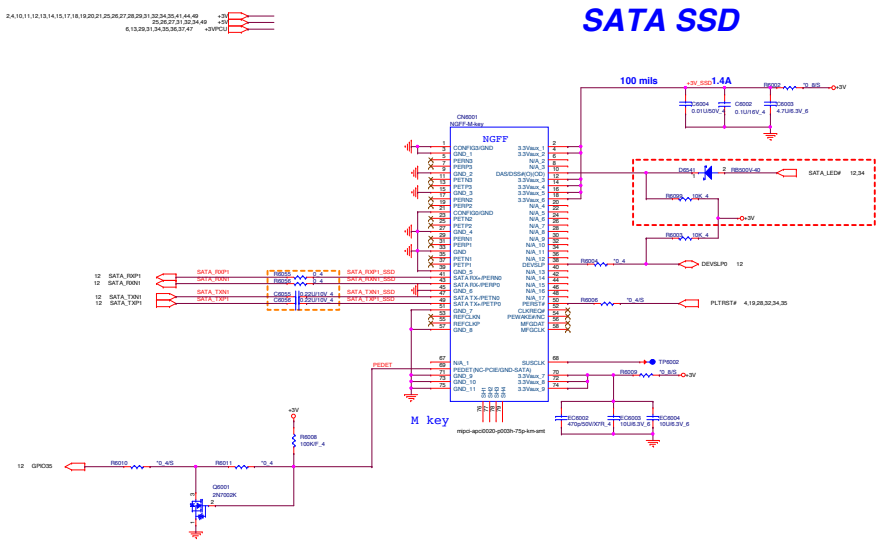
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	34 -- TPM/G-Sensor/IR CAM	1A

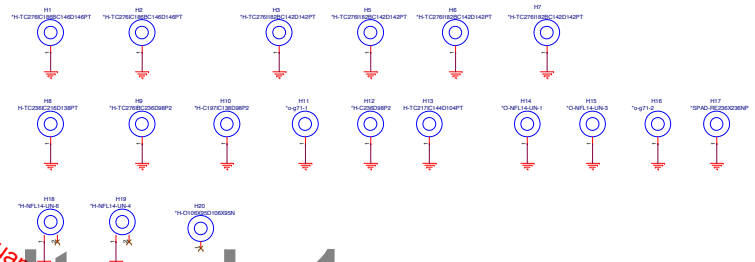
Date: Tuesday, December 13, 2016 | Sheet 32 of 49

SATA SSD



SATA ODD

Screw Hole



eMMC

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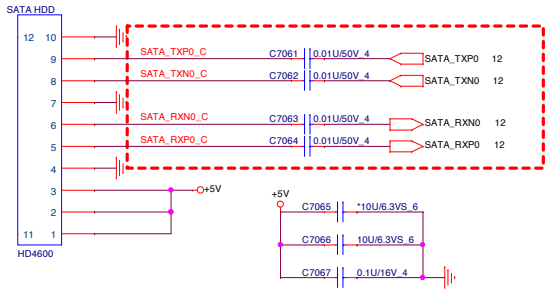
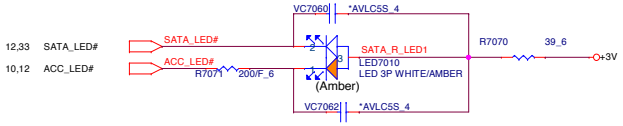
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size: Custom | Document Number: 35 – SSD_ODD_EMMC_ASM1152 | Rev: 1A
Date: Tuesday, December 13, 2016 | Sheet 33 of 49

HDD

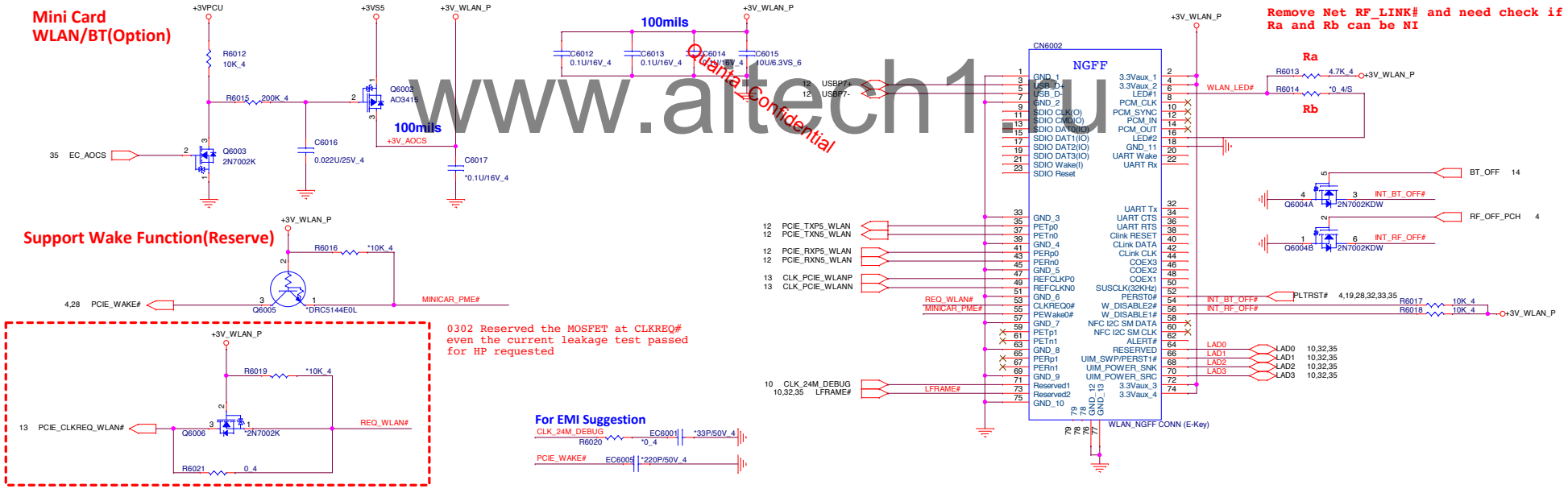
SATA HDD



SATA LED



WLAN



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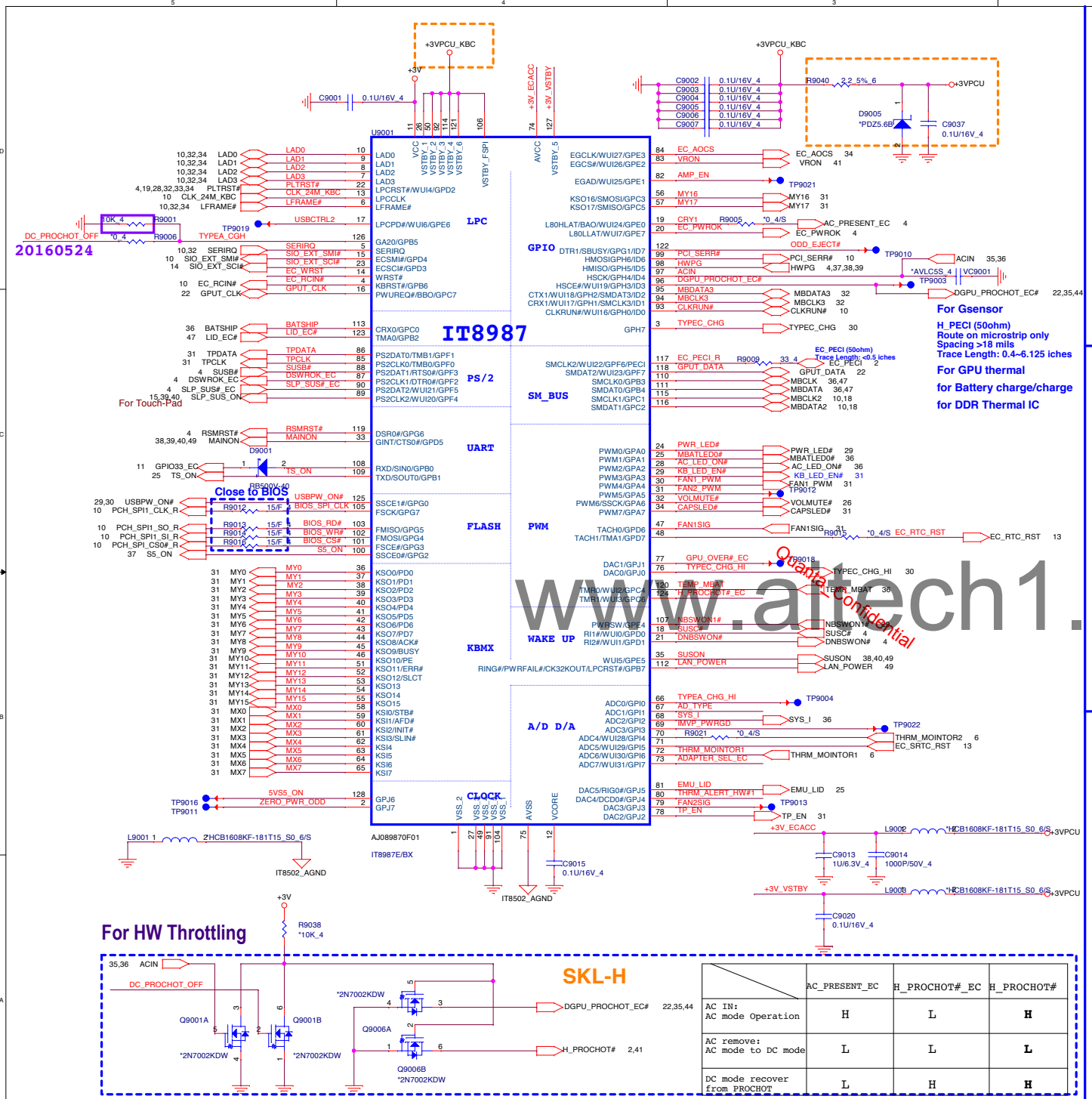
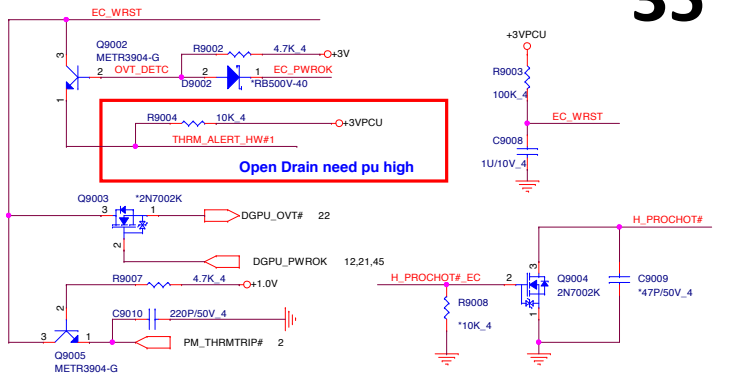
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size Custom	Document Number 36 -- HDD/WLAN(NGFF)	Rev 1A
Date: Tuesday, December 13, 2016	Sheet 34 of 49	



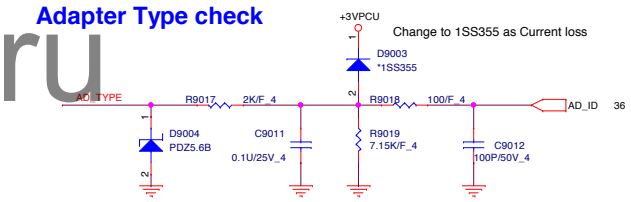
	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

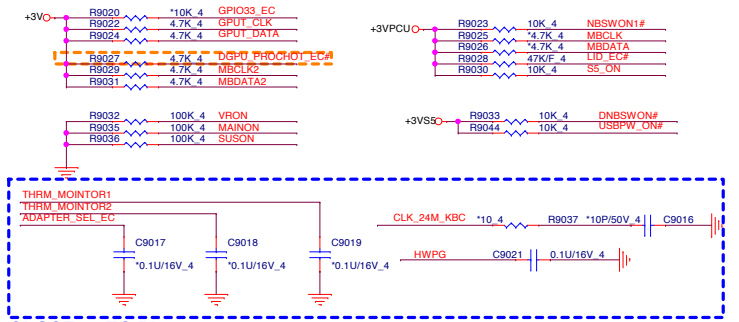


Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W				
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	3V	
120W	10K(CS31002FB26)		2.25V	
90W	10K(CS31002FB26)		1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB0)	0.75V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

Adapter Type check





CLOSE to EC Pin

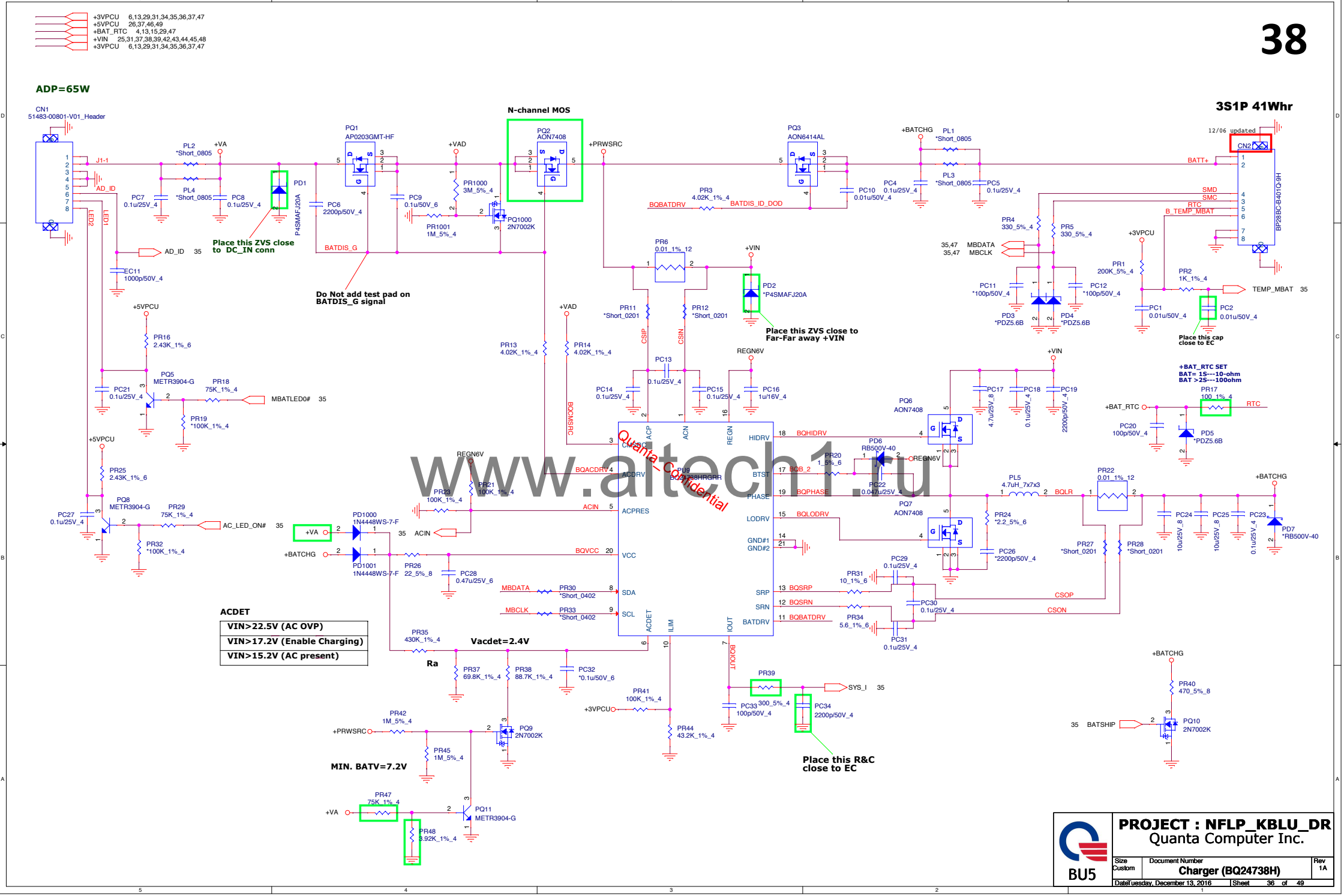
2,4,10,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,41,44,49 +3V
4,10,15,34,37,38,39,40,46,49 +3VS5
6,13,29,31,34,36,37,47 +3VPCU

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	37 -- EC (IT8987)	1A

Date: Tuesday, December 13, 2016 | Sheet 35 of 49


+3VPCU 6,13,29,31,34,35,36,37,47
+5VPCU 26,37,46,49
+BAT_RTC 4,13,15,29,47
+VIN 25,31,37,38,39,42,43,44,45,48
+3VPCU 6,13,29,31,34,35,36,37,47
ADP=65W
3S1P 41Whr
N-channel MOS
CN1 51483-00801-V01_Header
CN2 BP28BC-B401Q-9H
12/06 updated
Place this ZVS close to DC_IN conn
Do Not add test pad on BATDIS_G signal
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
+BAT_RTC SET
BAT= 1S---10-ohm
BAT >2S---100ohm
Vacdet=2.4V
Ra
MIN. BATV=7.2V
Place this R&C close to EC
ACDET
VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)
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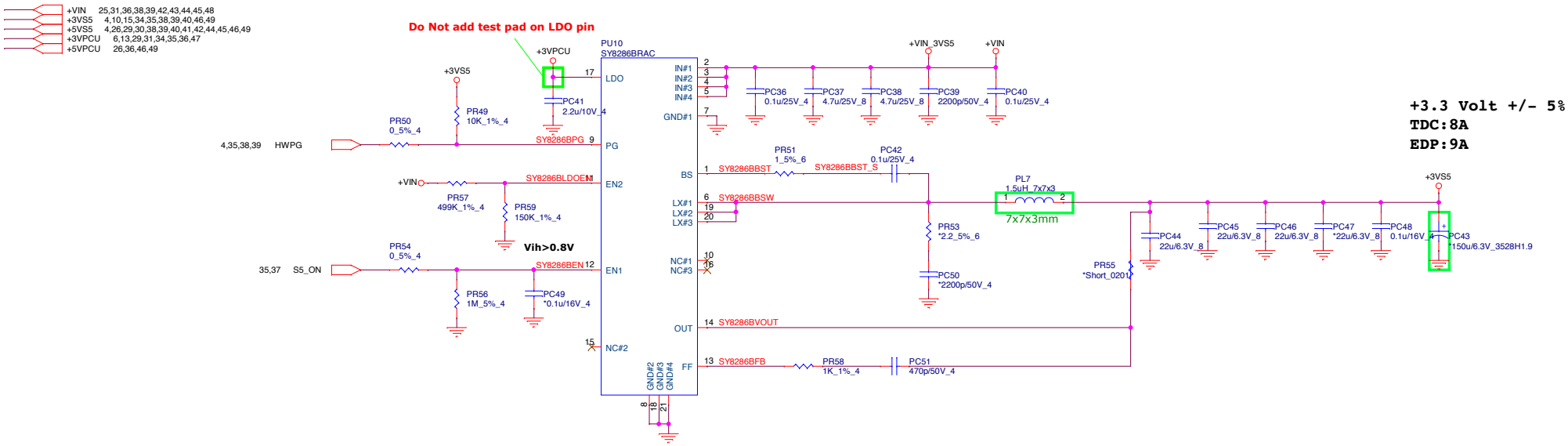
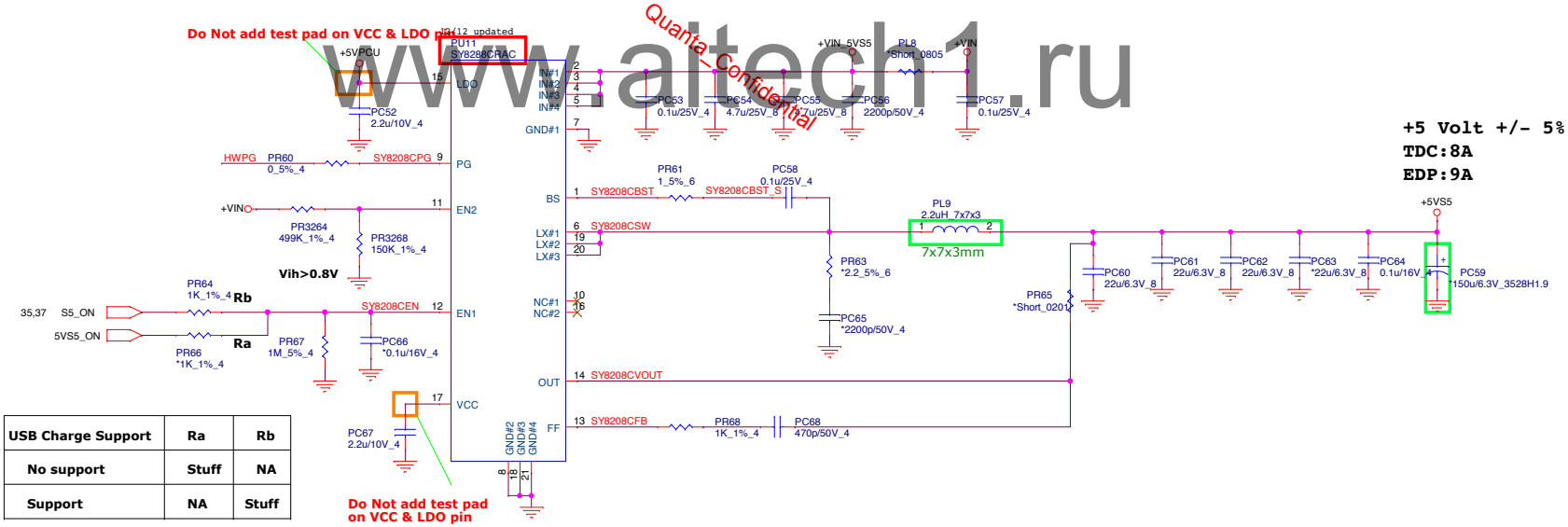
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size Custom
Document Number
Charger (BQ24738H)
Rev 1A
DateTuesday, December 13, 2016
Sheet 36 of 49

DC/DC +3VS5/+5VS5





USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

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PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A

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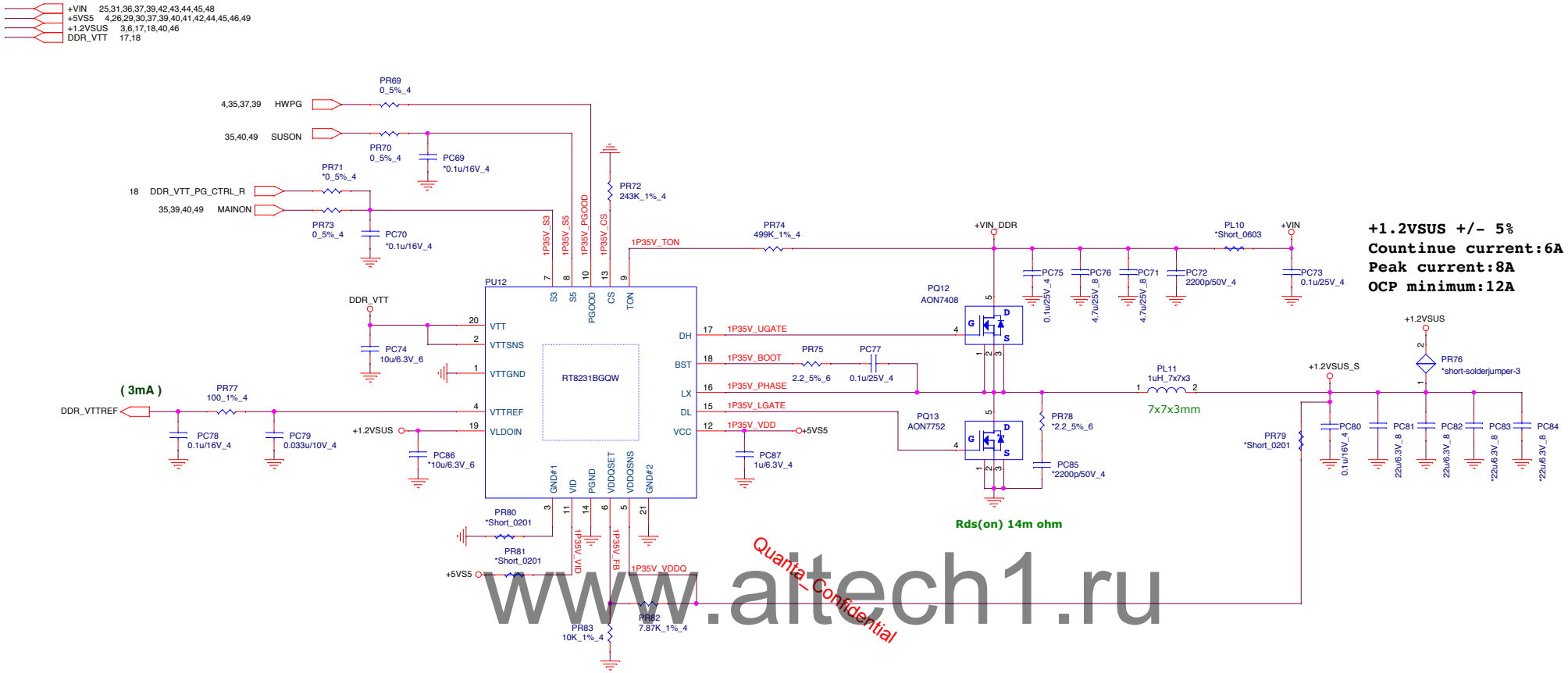

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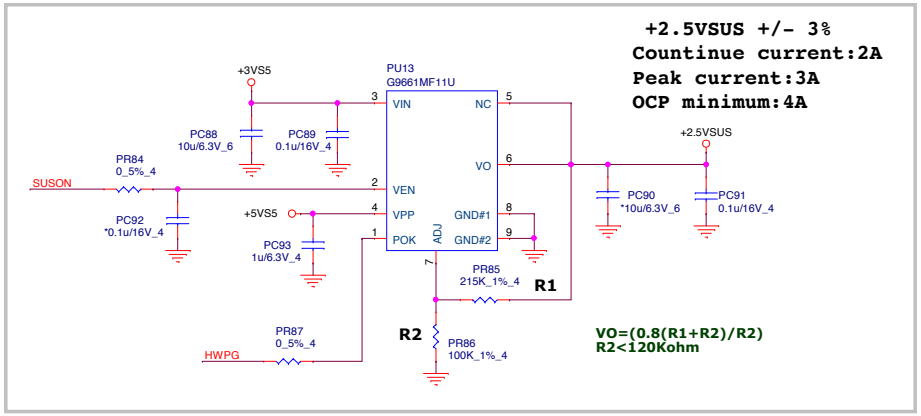
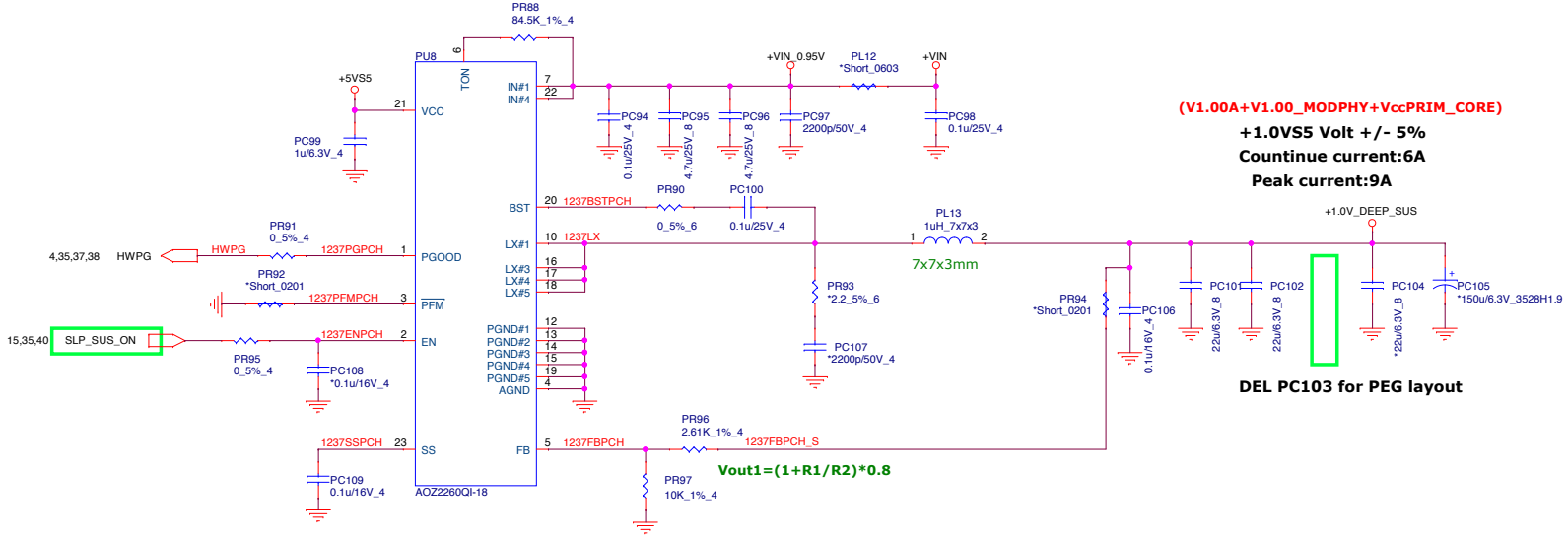
20151015 updated



BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size	Document Number DDR4 (G5619RZ1U)	Rev 1A
Date:Tuesday, December 13, 2016	Sheet 38 of 49	

+VIN 25,31,36,37,38,42,43,44,45,48
+3VS5 4,10,15,34,35,37,38,40,46,49
+5VS5 4,26,29,30,37,38,40,41,42,44,45,46,49
+1.0V_DEEP_SUS 9,13,15,40
+1.8V_DEEP_SUS 9,15
MAINON 35,38,39,40,49
+1.5V



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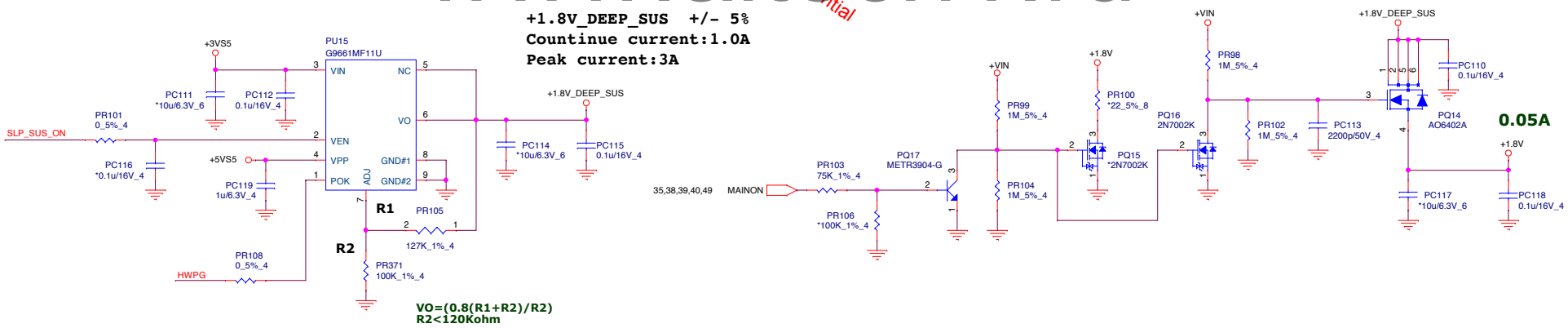


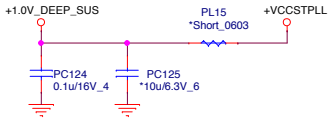
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size Custom	Document Number +1.0V/+1.8V_DEEP_SUS	Rev 1A
Date: Tuesday, December 13, 2016	Sheet 39 of 49	

+1.0V 2,4,6,35
+3VS5 4,10,15,34,35,37,38,39,46,49
+5VS5 4,26,29,30,37,38,39,41,42,44,45,46,49
+VCCIO 2,6
+1.2VSUS 3,6,17,18,38,46
+VCCSTPLL 2,4,5,6,9,41
+1.0V_DEEP_SUS 9,13,15,39
+1.2V_VCCPLL_OC 6
MAINON 35,38,39,49

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

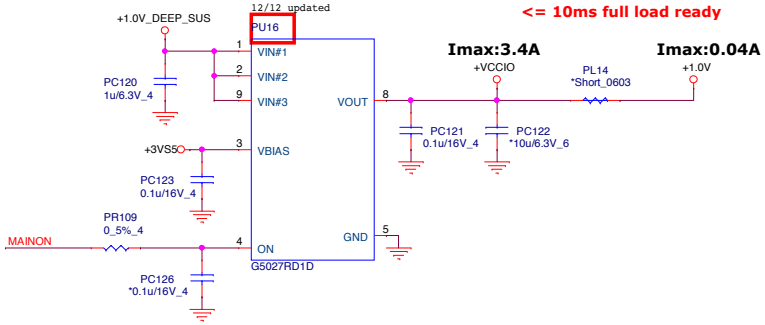
<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

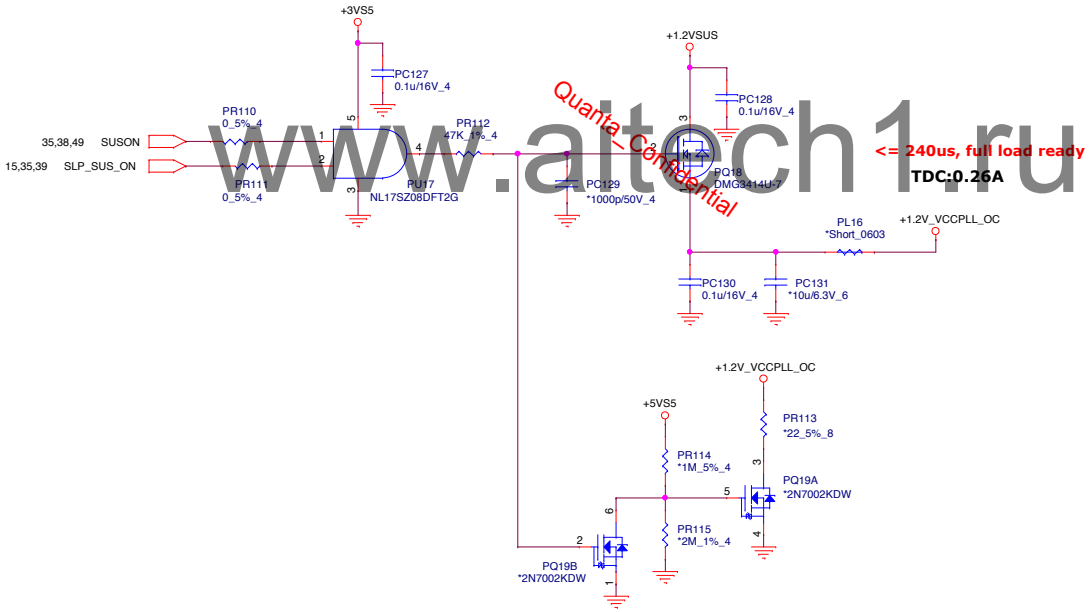
Imax:0.24A



Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready





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PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A

BU5

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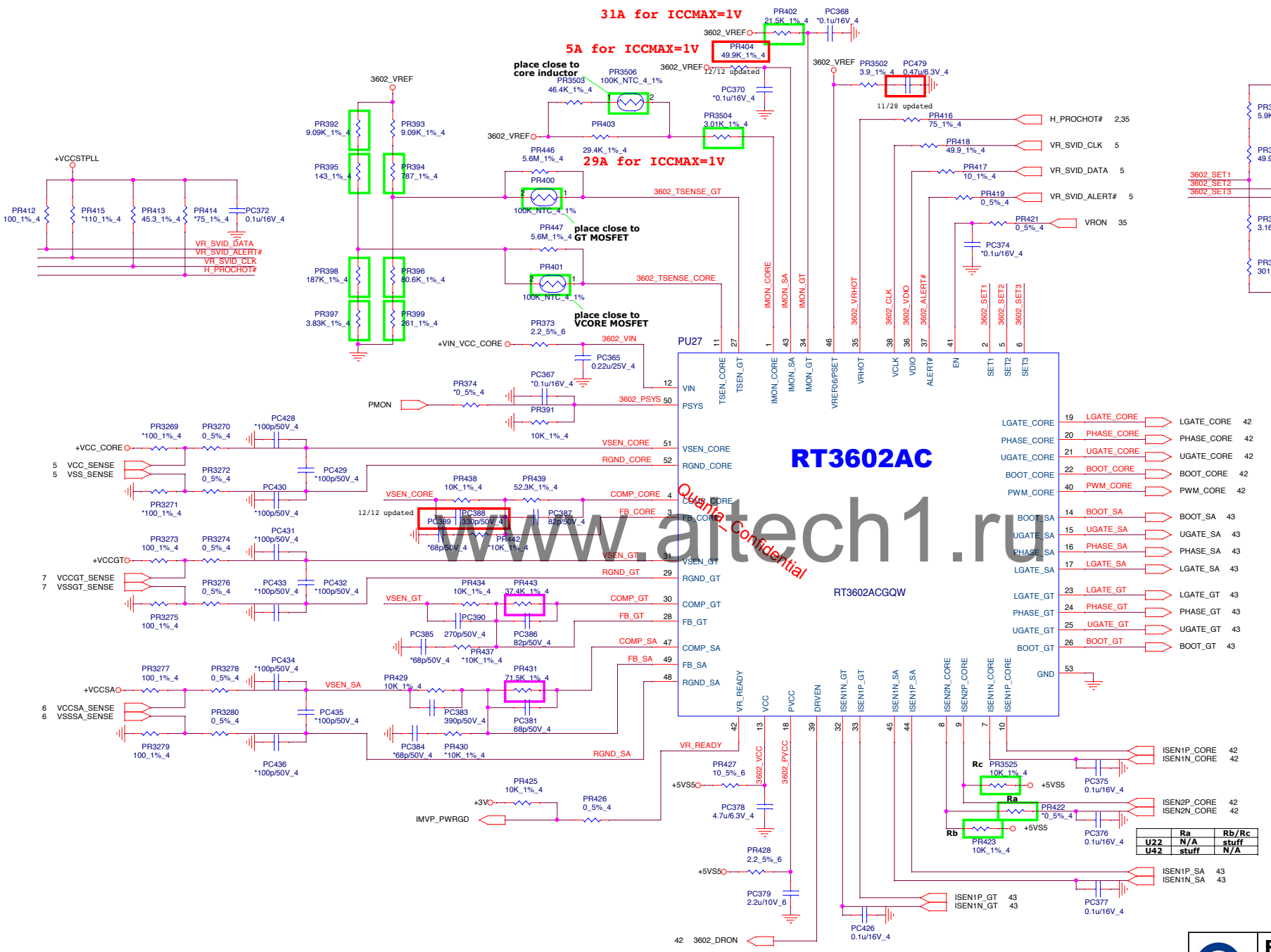

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	Ra	Rb/Rc
U22	N/A	stuff
U42	stuff	N/A

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU VR IC (RT3602AC)	2A

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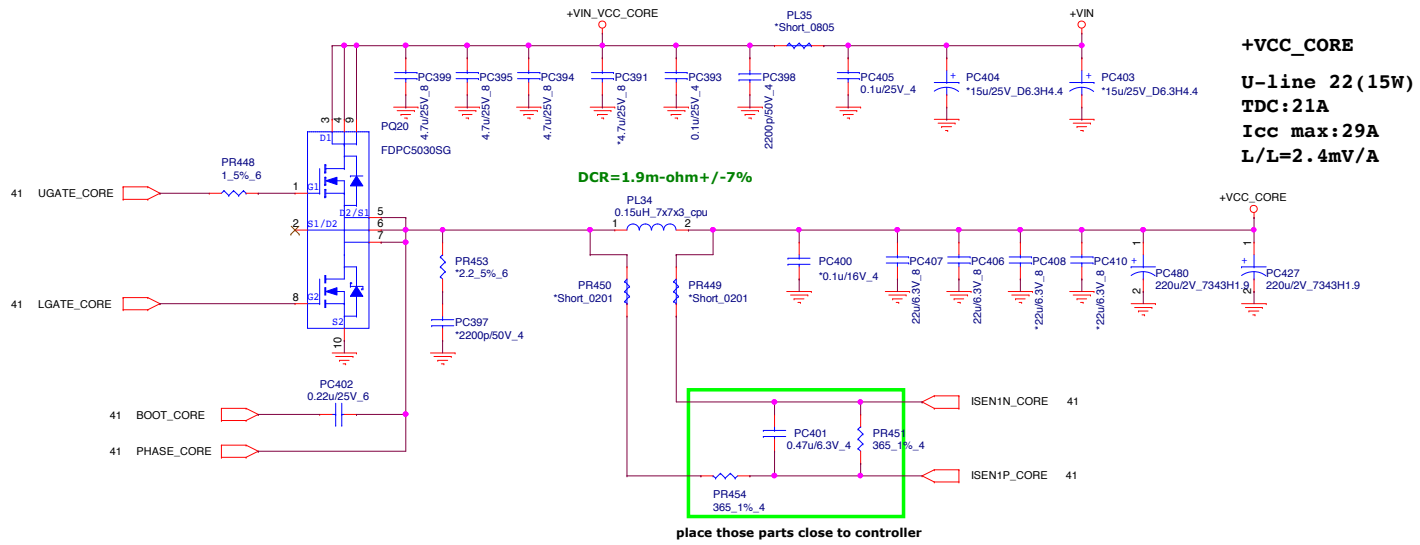
BU5

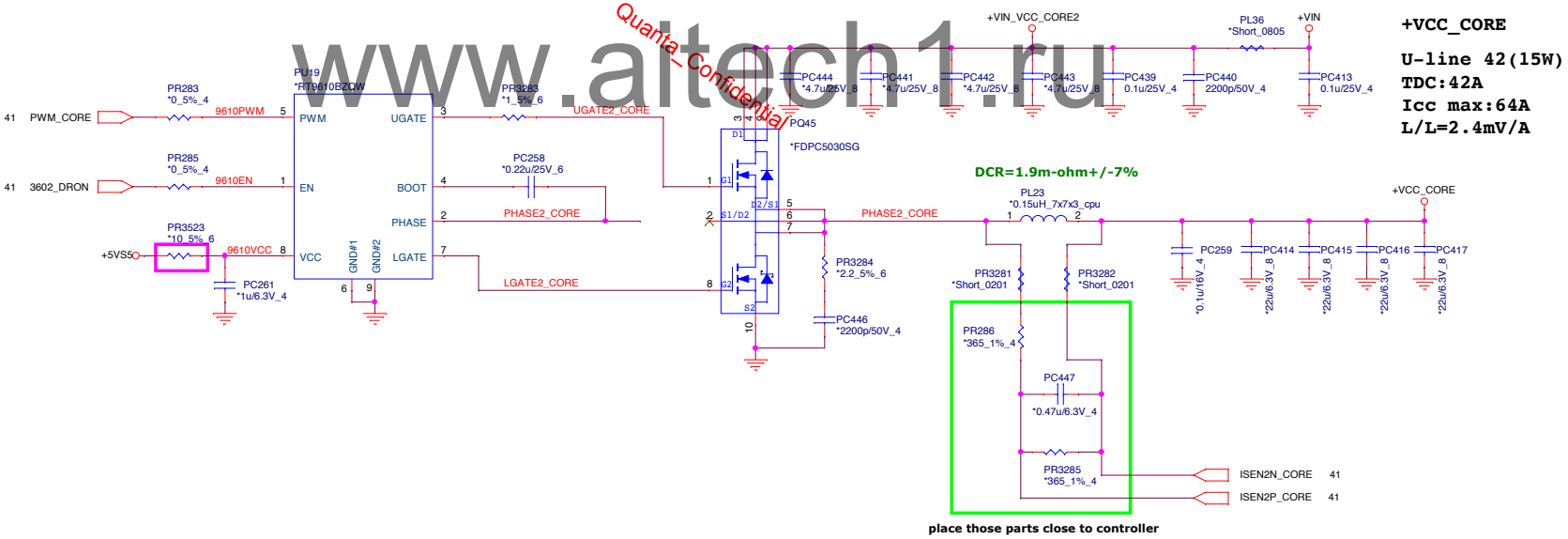
+VIN 25,31,36,37,38,39,43,44,45,48
+5VS5 4,26,29,30,37,38,39,40,41,44,45,46,49



+VCC_CORE

U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

For U42 --> Add These Components



+VCC_CORE

U-line 42(15W)
TDC:42A
Icc max:64A
L/L=2.4mV/A

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BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A

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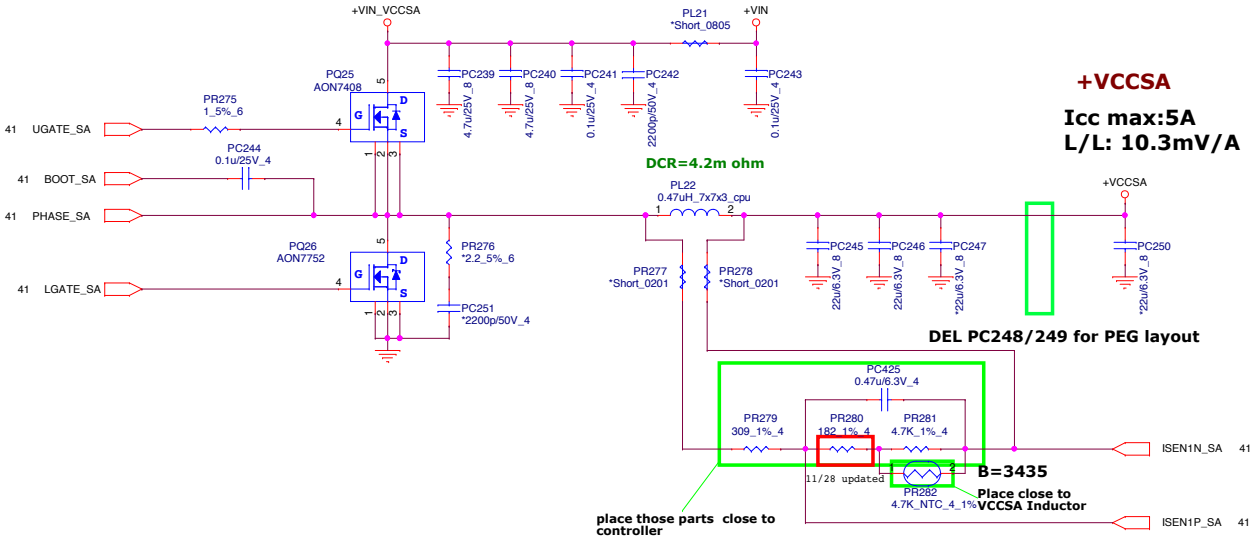
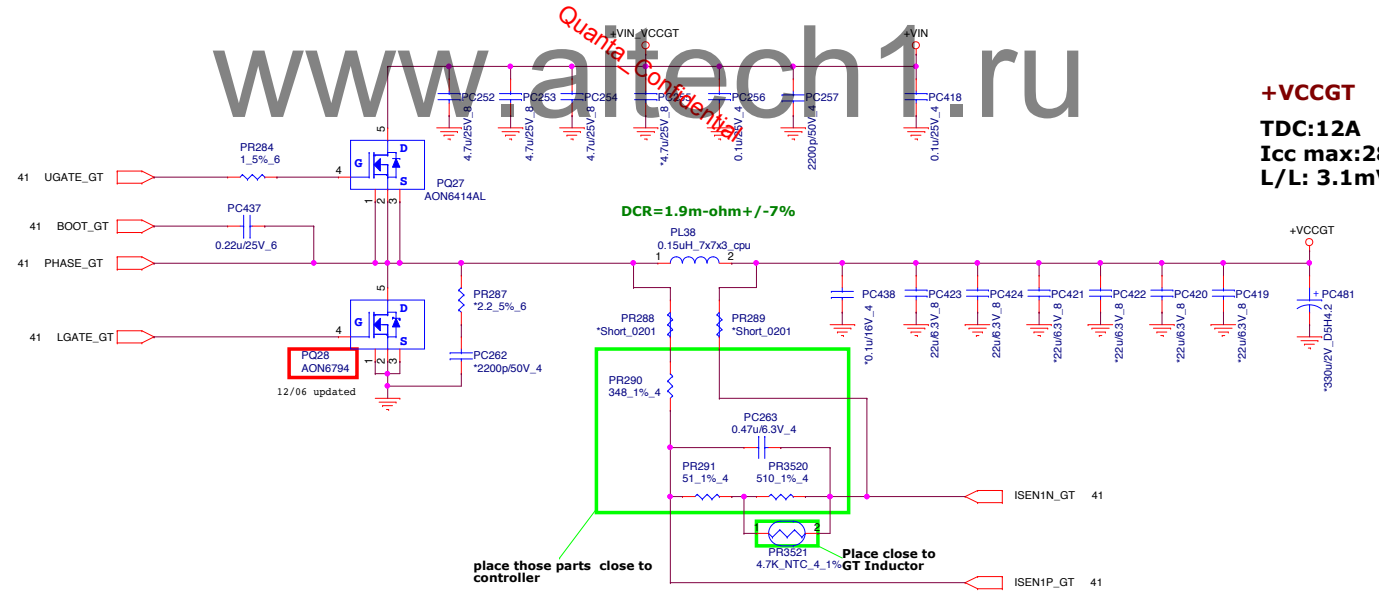
+VIN 25,31,36,37,38,39,42,44,45,48
+5VS5 4,26,29,30,37,38,39,40,41,42,44,45,46,49
+VCCSA 6,41
+VCCGT 7,41



+VCCSA

Icc max:5A
L/L: 10.3mV/A



+VCCGT

TDC:12A
Icc max:28A
L/L: 3.1mV/A

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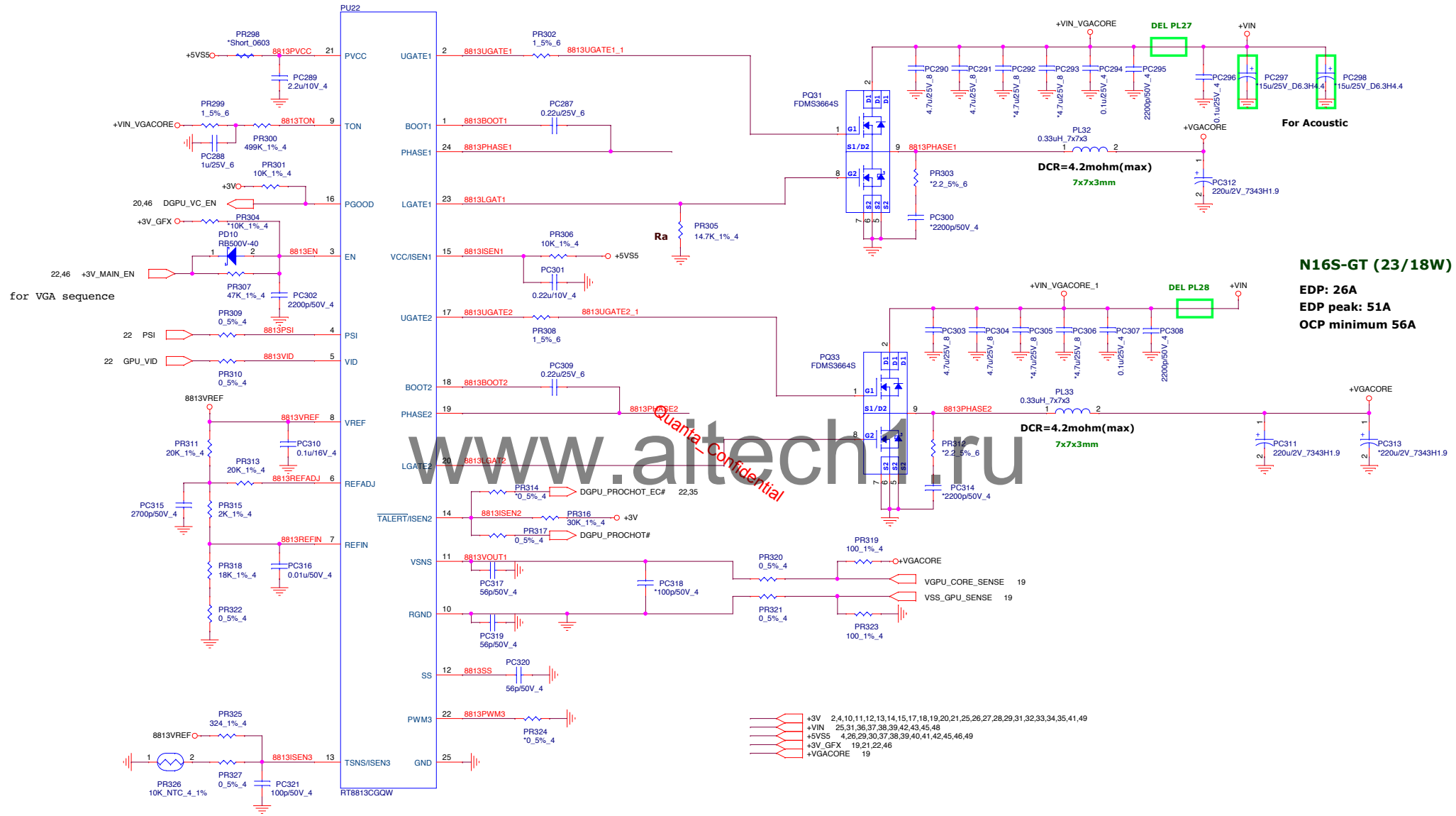
BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size Custom	Document Number +VCCSA (NCP81253)	Rev 2A
Date: Tuesday, December 13, 2016	Sheet 43 of 49	

VGA Core



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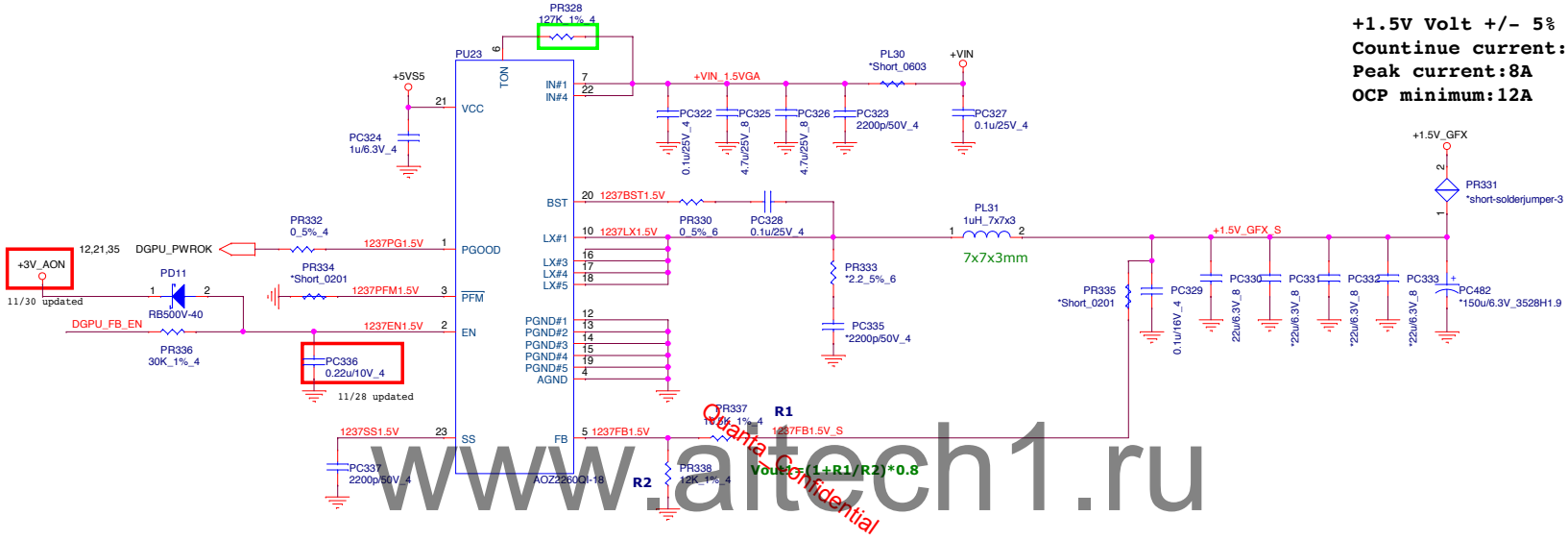
BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size Custom	Document Number **+VGACORE (RT8813C)**	Rev 2A
Date: Tuesday, December 13, 2016	Sheet 44 of 49	

+VIN 25,31,36,37,38,39,42,43,44,48
+5VS5 4,26,29,30,37,38,39,40,41,42,44,46,49
+1.5V_GFX 20,23,24

+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



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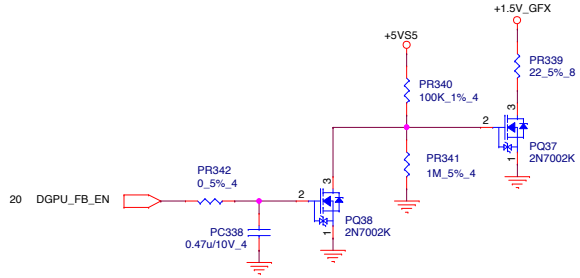
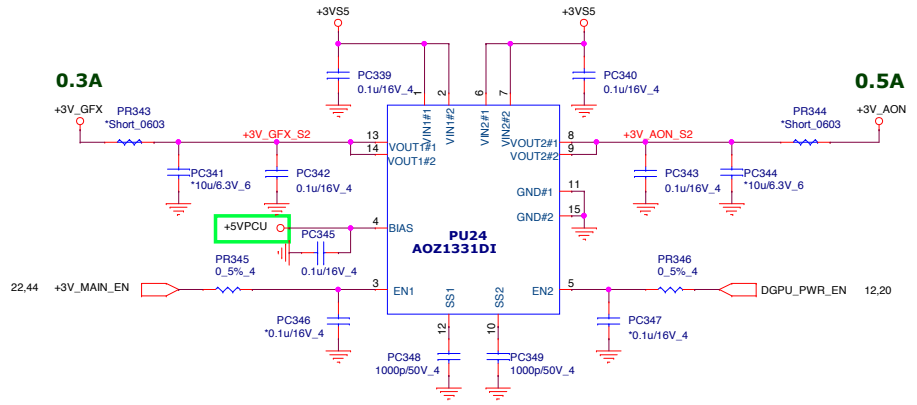
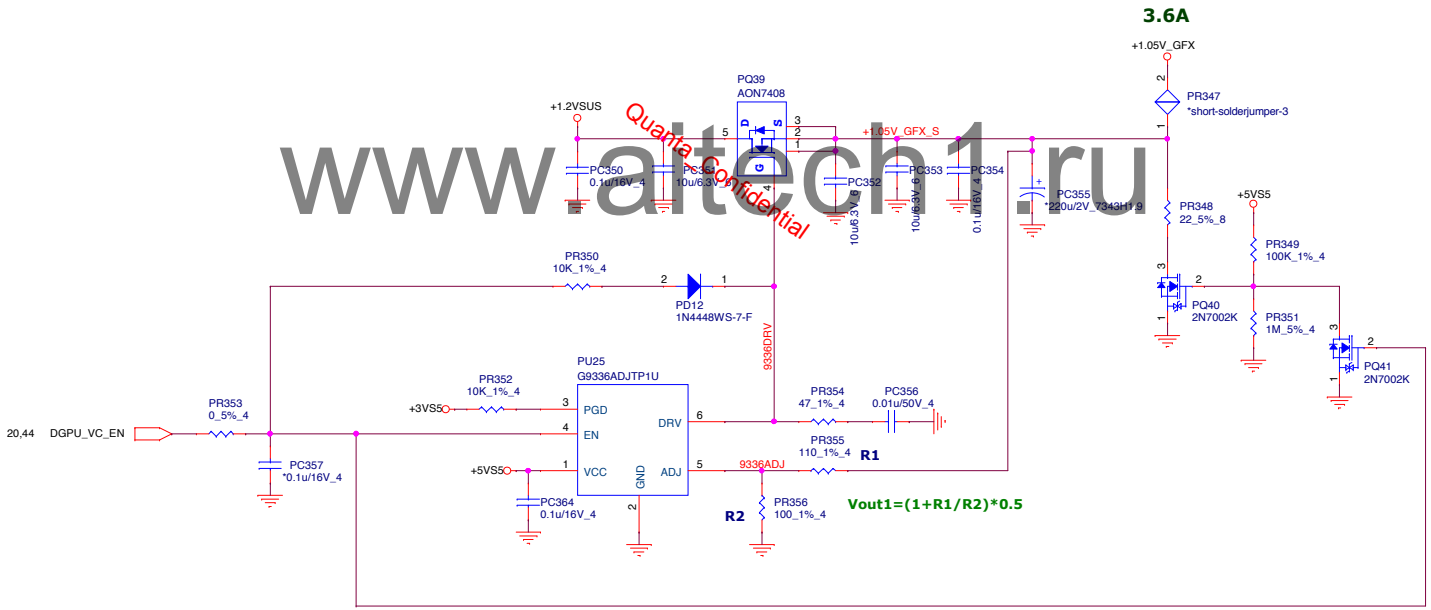


BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size Custom	Document Number **+1.5V_GFX (AOZ2260QI-18)**	Rev 1A
Date: Tuesday, December 13, 2016	Sheet 45 of 49	

+VIN 25,31,36,37,38,39,42,43,44,45,48
+3VS5 4,10,15,34,35,37,38,39,40,49
+5VS5 4,26,29,30,37,38,39,40,41,42,44,45,49
+3V_GFX 19,21,22,44
+3V_AON 19,22,45
+1.2VSUS 3,6,17,18,38,40
+1.05V_GFX 19,20,21





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BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(APL3523A)	1A

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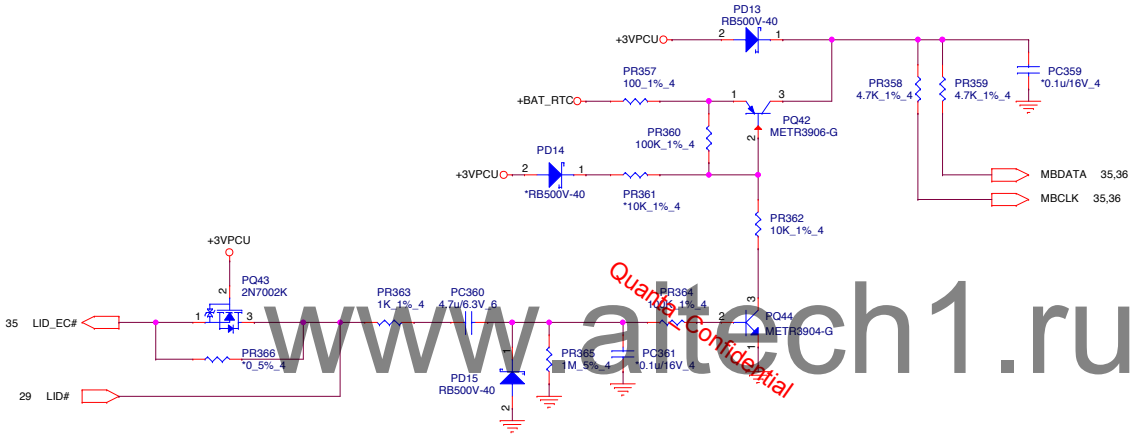
+3VPCU 6,13,29,31,34,35,36,37
+BAT_RTC 4,13,15,29,36



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PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LID SW for storage mode	1A

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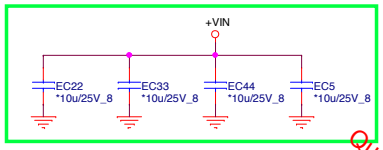
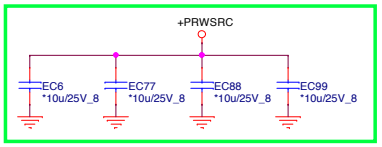
EMI request for ISN



EMI request for ISN



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BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size Custom	Document Number **EMI solution**	Rev 1A
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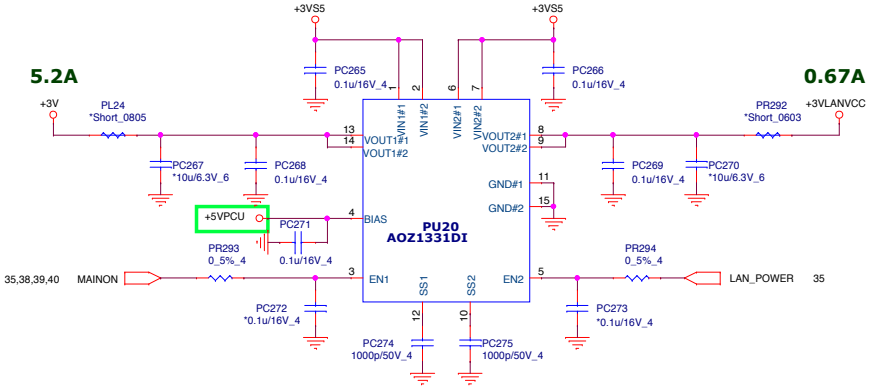
+3V 2,4,10,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44
+5V 25,26,27,31,32,34
+VIN 25,31,36,37,38,39,42,43,44,45,48
+3VS5 4,10,15,34,35,37,38,39,40,46
+5VS5 4,26,29,30,37,38,39,40,41,42,44,45,46
+3VSUS 31
+5VPCU 26,36,37,46
+3VLANVCC 28



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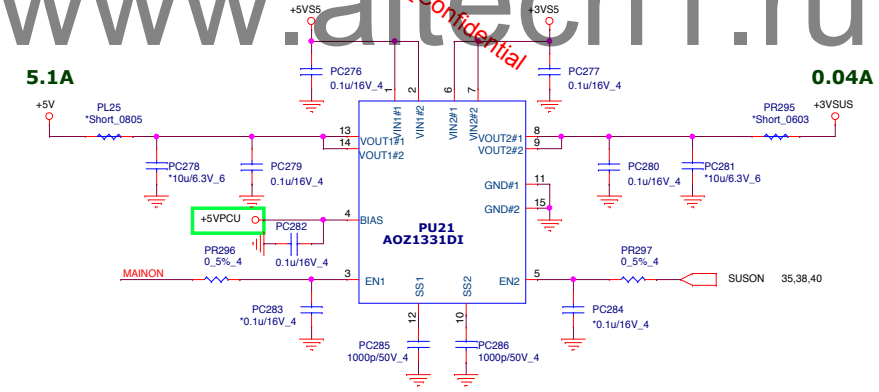

BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
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